



## 19. Course Specification of Logic Circuits I

<b>I. Course Identification and General Information:</b>						
1.	Course Title:	Logic Circuits I				
2.	Course Code & Number:	CCE111				
3.	Credit hours:	C.H				TOTAL
		Th.	Tut.	Pr.	Tr.	
		2	-	2	-	3
4.	Study level/ semester at which this course is offered:	2 <sup>nd</sup> Level/1 <sup>st</sup> Semester				
5.	Pre –requisite (if any):	Computer skills (UR003)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered:	Computer Engineering and Control				
8.	Language of teaching the course:	English				
9.	Location of teaching the course:	Faculty of Engineering				
10.	Prepared By:	Asst. Prof. Dr. Osama Al-Shibami				
11.	Date of Approval					

<b>II. Course Description:</b>
<p>This course aims to provide students with logic-algebra and digital system principles related to logic design and its applications in digital integrated circuits and systems. Course topics <b>include</b>; Number systems, binary arithmetic and codes, logic gates, Boolean algebra and logic simplifications, systematic design and realization of combinational circuits, Functions of combinational circuits logic using NAND and NOR gates. Throughout hands on work on logic lab, computer lab using simulation tools and term-projects for solving some simple practical problems to markets and industries, students will develop their practical and problem-solving skills in the field of digital system design and implementation.</p>

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



III. Course Intended learning outcomes (CILOs) of the course		Referenced PILOs
a1.	Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.	A1
a2.	Explain digital system, components or process to meet desired needs within realistic constraints.	A3
b1.	Identify engineering problems in the area of digital logic circuit design.	B2
b2.	Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.	B3, B4
c1.	Design of digital logic circuits using apply knowledge of number systems, codes and Boolean algebra.	C2
c2.	Use the techniques, skills, and modern engineering tools necessary for engineering practice.	C3
d1.	Function on teams through digital circuit experiments and projects Works.	D1

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
a1- Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.	<ul style="list-style-type: none"> <li>- Active Lectures,</li> <li>- Hands on Lab Work,</li> <li>- Presentation</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- Homework</li> <li>- Written Exam</li> <li>- Lab Assessments.</li> </ul>

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



<b>a2-</b> Explain digital system, components or process to meet desired needs within realistic constraints.	<ul style="list-style-type: none"> <li>- Lecture</li> <li>- Presentation</li> <li>- Class Discussion</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- Home Work</li> <li>- Written Exam.</li> </ul>
--	---	---

**(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies:**

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
<b>b1-</b> Identify engineering problems in the area of digital logic circuit design.	<ul style="list-style-type: none"> <li>- Active Lectures,</li> <li>- Projects,</li> <li>- Class Discussion</li> <li>- Problem Solving</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- Project Presentations,</li> <li>- <b>Homework</b></li> <li>- Written Exam.</li> </ul>
<b>b2-</b> Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.	<ul style="list-style-type: none"> <li>- Active Lectures,</li> <li>- Problem Solving</li> <li>- Hands-on Laboratory Work</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- <b>Homework</b></li> <li>- Written Exam,</li> <li>- Lab Assessments.</li> </ul>

**(C) Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies:**

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
<b>c1-</b> <b>Design</b> digital logic circuits using apply knowledge of number systems, codes and Boolean algebra.	<ul style="list-style-type: none"> <li>- Active Lectures,</li> <li>- Presentation</li> <li>- Class Discussion</li> <li>- Problem Solving</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- <b>Homework</b></li> <li>- Written Exam.</li> </ul>
<b>c2-</b> and Use the techniques, skills, modern engineering tools necessary for engineering practice.	<ul style="list-style-type: none"> <li>- Hands on Lab Work,</li> <li>- Computer-based Lab Works,</li> <li>- Presentation</li> <li>- Problem Solving</li> </ul>	<ul style="list-style-type: none"> <li>- Quizzes</li> <li>- Lab Assessments,</li> <li>- Lab Reports</li> <li>- <b>Homework</b></li> <li>- Written Exam.</li> </ul>

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



<b>(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies:</b>		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
<b>d1-</b> Function on teams through digital circuit experiments and projects works.	- Lab Work - Class Discussion	- Quizzes - <b>Homework</b> - Projects Presentations, - Lab Reports.

<b>IV. Course Content:</b>					
<b>A – Theoretical Aspect:</b>					
Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	Contact hours
1.	Introduction to Logic Circuits and its applications	a1, a2	<ul style="list-style-type: none"> <li>Analog and Digital Systems</li> <li>Binary Digits and Logic Levels</li> <li>Digital Waveforms</li> <li>Timing Diagrams</li> <li>Serial and Parallel Data</li> <li>Basic Logic Functions</li> <li>Programmable Logic</li> <li>Logic CAD system (VHDL)</li> </ul>	1	2
2.	Number systems and Codes	a2, b1, b2, c1	<ul style="list-style-type: none"> <li>Binary, Octal and Hex Number Systems</li> <li>Number Systems Conversions.</li> <li>BCD, Gray and Alphanumeric Codes.</li> </ul>	1	2

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



			<ul style="list-style-type: none"> <li>Error Detection.</li> </ul>		
3.	Digital Arithmetic	a2, b1, b2, c1	<ul style="list-style-type: none"> <li>Un-Signed, Signed Numbers Representations,</li> <li>1's &amp; 2's Complements Number Representations, and Scientific Representations,</li> <li>Binary addition and Subtraction: effective of 2's Complements on subtraction operation,</li> <li>Binary Multiplication and Division.</li> <li>BCD Addition and Hex. Arithmetic</li> </ul>	3	6
4.	Logic Gates	a1, a2, b1, b2, c1,	<ul style="list-style-type: none"> <li>Boolean Constants and Variables.</li> <li>Truth Tables.</li> <li>OR, AND, and NOT Operations.</li> <li>Logic Algebra and Logic Implementation.</li> <li>NOR and NAND Gates</li> </ul>	2	4
5.	Boolean Algebra and Logic Simplification	a1, a2, b1, b2, c1	<ul style="list-style-type: none"> <li>Boolean and Demorgan's Theorems.</li> <li>Universality of NAND and NOR Gates.</li> <li>Alternative Representations.</li> <li>Labeling Logic Signals.</li> <li>SOP and POS Forms.</li> </ul>	2	4

Prepared by

Head of Department  
 Asst. Prof. Dr. Adel  
 Ahmed Al-Shakiri

Quality Assurance Unit  
 Assoc. Prof. Dr.  
 Mohammad Algorafi

Dean of the Faculty  
 Prof. Dr. Mohammed  
 AL-Bukhaiti

Academic Development  
 Center & Quality Assurance  
 Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



			<ul style="list-style-type: none"> <li>Simplifying Logic Circuits using algebra and K-maps.</li> </ul>		
6.	Combinational Logic	a1, a2, b1, b2, c1	<ul style="list-style-type: none"> <li>Introduction</li> <li>Basic Circuits and Design Procedure.</li> <li>Using NAND and NOR gates in Design.</li> <li>Display Devices</li> </ul>	1	2
7.	Combinational Circuits	a1, a2, b1, b2, c1	<ul style="list-style-type: none"> <li>Introduction.</li> <li>Arithmetic Circuits and Comparators.</li> <li>Decoders, and Encoders.</li> <li>Multiplexers and Demultiplexers.</li> </ul>	2	4
8.	Combinational Logic Programming	a1, a2, b1, b2, c1, c2	<ul style="list-style-type: none"> <li>Introduction</li> <li>Describing Logic circuits</li> <li>Development Software</li> <li>Description languages and Programming Languages</li> <li>Implementing Logic Circuits using PLDs</li> <li>VHDL Format and Syntax</li> <li>Intermediate signals in VHDL</li> <li>Representing Data in VHDL</li> <li>Truth Tables using VHDL</li> <li>Decision Control Structures</li> <li>Implementing Adders, Decoders, Encoders,</li> </ul>	2	4

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



			Multiplexers, Demultiplexers, Magnitude Comparators, Code Converters.		
<b>Number of Weeks /and Units Per Semester</b>				<b>14</b>	<b>28</b>

<b>B - Practical Aspect:</b>				
<b>Order</b>	<b>Tasks/ Experiments</b>	<b>Number of Weeks</b>	<b>Contact hours</b>	<b>Learning Outcomes</b>
1.	AND with 2 Inputs and 3 Inputs	1	2	b1, b2, c1, c2, d1
2.	OR with 2 Inputs and 3 Inputs	1	2	b1, b2, c1, c2, d1
3.	NAND with 2 Inputs and 3 Inputs	1	2	b1, b2, c1, c2, d1
4.	NOR with 2 Inputs and 3 Inputs	1	2	b1, b2, c1, c2, d1
5.	XOR and XNOR	1	2	b1, b2, c1, c2, d1
6.	XOR by using NAND gates	1	2	b1, b2, c1, c2, d1
7.	XOR by using NOR gates	1	2	b1, b2, c1, c2, d1
8.	Decoder	1	2	b1, b2, c1, c2, d1
9.	Decoder with 7 segments	1	2	b1, b2, c1, c2, d1
10.	Encoder	1	2	b1, b2, c1, c2, d1

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



11.	Multiplexer	1	2	b1, b2, c1, c2, d1
12.	Demultiplexer	1	2	b1, b2, c1, c2, d1
13.	Review	1	2	a1, a2, b1, b2, c1, c2, d1
14.	Final Submission of Projects Reports and Presentations: Students work in groups of 2 or 3 students to solve some practical problems	1 (Starting from Week No.4)	2	a1, a2, b1, b2, c1, c2, d1
<b>Number of Weeks /and Units Per Semester</b>		<b>14</b>	<b>28</b>	

### V. Teaching strategies of the course:

- Active Lectures,
- Hands on Lab Work,
- Computer-based Lab Work,
- Class Discussion
- Problem Solving
- Projects & Presentations

### VI. Assignments & Reports:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	Number Systems and their Arithmetic	a1, a2, b1	3 <sup>rd</sup> & 4 <sup>th</sup>	3
2.	Boolean Algebra & K-Map Simplifications with lab Report.	a1, a2, b1, b2, d1	6 <sup>th</sup> & 9 <sup>th</sup>	6

Prepared by

Head of Department  
 Asst. Prof. Dr. Adel  
 Ahmed Al-Shakiri

Quality Assurance Unit  
 Assoc. Prof. Dr.  
 Mohammad Algorafi

Dean of the Faculty  
 Prof. Dr. Mohammed  
 AL-Bukhaiti

Academic Development  
 Center & Quality Assurance  
 Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas





3.	Combinational Logic Circuits Design (Adders, Sub, Multipliers, Divisions, Comparators, MUXs. & Decoders) with lab Reports.	a1, a2, b1, b2, c1, d1	10 <sup>th</sup> to 13 <sup>th</sup>	6
<b>Total Marks</b>				<b>15</b>

<b>VII. Schedule of Assessment Tasks for Students During the Semester:</b>					
No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & Reports	3 <sup>rd</sup> to 13 <sup>th</sup>	15	10%	a1, a2, b1, b2, c1, d1
2.	Quizzes	5 <sup>th</sup> , 10 <sup>th</sup> & 14 <sup>th</sup>	10	6.67%	a1, a2, b1, b2
3.	Midterm Exam (Theory)	8 <sup>th</sup>	20	13.33%	a1, a2, b1, b2, c1
4.	Final Lab. Exam (including Course Project Evaluation)	14 <sup>th</sup> & 15 <sup>th</sup>	30	20%	a1, a2, b1, b2, c1, d1
5.	Final Exam (Theory)	16 <sup>th</sup>	75	50%	a1, a2, b1, b2, c1, c2
<b>Total Marks / Percentage</b>			<b>150</b>	<b>100%</b>	

<b>VIII. Learning Resources:</b>	
<ul style="list-style-type: none"> <li>• <i>Written in the following order: ( Author - Year of publication – Title – Edition – Place of publication – Publisher).</i></li> </ul>	
<b>1- Required Textbook(s) ( maximum two ).</b>	
1	1 -Thomas L. Floyd, 2009, Digital Fundamentals, 10 <sup>th</sup> Edition, Pearson Education International
2	2- Ronald J. Tocci, Neal S.Widmer, Gregory L. Moss, 2007, Digital Systems : Principles and Applications, 10 <sup>th</sup> Edition,. Pearson Prentice Hall
<b>2- Essential References.</b>	

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



	1-Douglas L. Perry, 2002, VHDL Programming by Example, 4 <sup>th</sup> Edition, McGraw-Hill 2 -M. M. Mano, M. D. Ciletti, 2007, Digital Design, 4 <sup>th</sup> Edition, Prentice-Hall
<b>3- Electronic Materials and Web Sites etc.</b>	
	1-Faculty Electronic Library

<b>IX. Course Policies:</b>	
1.	<b>Class Attendance:</b> -A student should attend not less than 75 % of total hours of the subject; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring <b>an approved</b> statement from university Clinic
2.	<b>Tardy:</b> - For late in attending the class, the student will be initially notified. If he repeated lateness in attending class he will be considered as absent.
3.	<b>Exam Attendance/Punctuality:</b> - A student should attend the exam on time. He is Permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam.
4.	<b>Assignments &amp; Projects:</b> - The assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time.
5.	<b>Cheating:</b> - For cheating in exam, a student will be considered as <b>failure</b> . In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.
6.	<b>Plagiarism:</b> Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee <b>proved</b> a plagiarism of a student, he will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university.
7.	<b>Other policies:</b>

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



	<ul style="list-style-type: none"> <li>- Mobile phones are not allowed to use during a class lecture. It must be closed, otherwise the student will be asked to leave the lecture room</li> <li>- Mobile phones are not allowed in class during the examination.</li> </ul> <p>Lecture notes and assignments my given directly to students using soft or hard copy</p>
--	--

<b>Reviewed By</b>	<p><b><u>Vice Dean for Academic Affairs and Post Graduate Studies: Asst. Prof. Dr. Tarek A. Barakat</u></b></p> <p><b><u>President of Quality Assurance Unit: Assoc. Prof. Dr. Mohammed Algorafi</u></b></p> <p><b><u>Name of Reviewer from the Department: Assoc. Prof. Dr. Farouk Al-Fuhaidy</u></b></p>
	<p><b><u>Deputy Rector for Academic Affairs Asst. Prof. Dr. Ibrahim AlMutaa</u></b></p> <p><b><u>Assoc. Prof. Dr. Ahmed Mujahed</u></b></p> <p><b><u>Asst. Prof. Dr. Munasar Alsubri</u></b></p>

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



## 19. Template for Course Plan of Logic Circuits 1

Information about Faculty Member Responsible for the Course:						
Name of Faculty Member	Dr. Osama Al-Shibami	Office Hours				
Location & Telephone No.	Electrical Eng. Dept.	SAT	SUN	MON	TUE	WED
E-mail	Alshibami@yemen.net				10-12	

II. Course Identification and General Information:						
1.	Course Title:	Logic Circuits I				
2.	Course Number & Code:	CCE111				
3.	Credit hours:	C.H				Total
		Th.	Tut.	Pr.	Tr.	
		2	-	2	-	
4.	Study level/year at which this course is offered:	2 <sup>nd</sup> Level/1 <sup>st</sup> Semester				
5.	Pre –requisite (if any):	Computer skills (UR003)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered	Computer Engineering and Control				
8.	Language of teaching the course:	English				
9.	System of Study:	Semester System				
10.	Mode of delivery:	Lecture				
11.	Location of teaching the course:	Classroom				

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



### III. Course Description:

This course aims to provide students with logic-algebra and digital system principles related to logic design and its applications in digital integrated circuits and systems. Course topics **include**; Number systems, binary arithmetic and codes, logic gates, Boolean algebra and logic simplifications, systematic design and realization of combinational circuits, Functions of combinational circuits logic using NAND and NOR gates. Throughout hands on work on logic lab, computer lab using simulation tools and term-projects for solving some simple practical problems to markets and industries, students will develop their practical and problem-solving skills in the field of digital system design and implementation.

### IV. Intended learning outcomes (ILOs) of the course:

- Brief summary of the knowledge or skill the course is intended to develop:
  1. Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.
  2. Explain digital system, components or process to meet desired needs within realistic constraints.
  3. Identify engineering problems in the area of digital logic circuit design.
  4. Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.
  5. **Design** digital logic circuits using **and applying** knowledge of number systems, codes and Boolean algebra.
  6. Use the techniques, skills, and modern engineering tools necessary for engineering practice.
  7. Function on teams through digital circuit experiments and projects works.

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



<b>V. Course Content:</b>				
<ul style="list-style-type: none"> <li>Distribution of Semester Weekly Plan of Course Topics/Items and Activities.</li> </ul>				
<b>A – Theoretical Aspect:</b>				
<b>Order</b>	<b>Topics List</b>	<b>Sub Topics List</b>	<b>Week Due</b>	<b>Contact Hours</b>
1.	Introduction to Logic Circuits and its applications	<ul style="list-style-type: none"> <li>Analog and Digital Systems</li> <li>Binary Digits and Logic Levels</li> <li>Digital Waveforms</li> <li>Timing Diagrams</li> <li>Serial and Parallel Data</li> <li>Basic Logic Functions</li> <li>Programmable Logic</li> <li>Logic CAD system (VHDL)</li> </ul>	1 <sup>st</sup>	2
2.	Number systems and Codes	<ul style="list-style-type: none"> <li>Binary, Octal and Hex Number Systems</li> <li>Number Systems Conversions.</li> <li>BCD, Gray and Alphanumeric Codes.</li> <li>Error Detection.</li> </ul>	2 <sup>nd</sup>	2
3.	Digital Arithmetic	<ul style="list-style-type: none"> <li>Un-Signed, Signed Numbers Representations,</li> <li>1's &amp; 2's Complements Number Representations, and Scientific Representations,</li> <li>Binary addition and Subtraction: effective of 2's Complements on subtraction operation,</li> <li>Binary Multiplication and Division.</li> <li>BCD Addition and Hex. Arithmetic</li> </ul>	3 <sup>rd</sup> , 4 <sup>th</sup> , 5 <sup>th</sup>	6

Prepared by Head of Department  
 Asst. Prof. Dr. Adel  
 Ahmed Al-Shakiri

Quality Assurance Unit  
 Assoc. Prof. Dr.  
 Mohammad Algorafi

Dean of the Faculty  
 Prof. Dr. Mohammed  
 AL-Bukhaiti

Academic Development  
 Center & Quality Assurance  
 Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



4.	Logic Gates	<ul style="list-style-type: none"> <li>• Boolean Constants and Variables.</li> <li>• Truth Tables.</li> <li>• OR, AND, and NOT Operations.</li> <li>• Logic Algebra and Logic Implementation.</li> <li>• NOR and NAND Gates</li> </ul>	6 <sup>th</sup> , 7 <sup>th</sup>	4
5.	Mid Term Exam		8 <sup>th</sup>	2
6.	Boolean Algebra and Logic Simplification	<ul style="list-style-type: none"> <li>• Boolean and Demorgan's Theorems.</li> <li>• Universality of NAND and NOR Gates.</li> <li>• Alternative Representations.</li> <li>• Labeling Logic Signals.</li> <li>• SOP and POS Forms.</li> <li>• Simplifying Logic Circuits using algebra and K-maps.</li> </ul>	9 <sup>th</sup> , 10 <sup>th</sup>	4
7.	Combinational Logic	<ul style="list-style-type: none"> <li>• Introduction</li> <li>• Basic Circuits and Design Procedure.</li> <li>• Using NAN and NOR gates in Design.</li> <li>• Display Devices</li> </ul>	11 <sup>th</sup>	2
8.	Combinational Circuits	<ul style="list-style-type: none"> <li>• Introduction.</li> <li>• Arithmetic Circuits and Comparators.</li> <li>• Decoders, and Encoders.</li> <li>• Multiplexers and Demultiplexers.</li> </ul>	12 <sup>th</sup> , 13 <sup>th</sup>	4
9.	Combinational Logic Programming	<ul style="list-style-type: none"> <li>• Introduction</li> <li>• Describing Logic circuits</li> <li>• Development Software</li> <li>• Description languages and Programming Languages</li> <li>• Implementing Logic Circuits using PLDs</li> </ul>	14 <sup>th</sup> , 15 <sup>th</sup>	4

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



		<ul style="list-style-type: none"> <li>VHDL Format and Syntax</li> <li>Intermediate signals in VHDL</li> <li>Representing Data in VHDL</li> <li>Truth Tables using VHDL</li> <li>Decision Control Structures</li> <li>Implementing Adders, Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators, Code Converters.</li> </ul>		
10.	Final Exam		16 <sup>th</sup>	2
<b>Number of Weeks /and Units Per Semester</b>			<b>16</b>	<b>32</b>

<b>B – Practical Aspect:</b>			
Order	Topics List	Week Due	Contact Hours
1.	AND with 2 Inputs and 3 Inputs	1 <sup>st</sup>	2
2.	OR with 2 Inputs and 3 Inputs	2 <sup>nd</sup>	2
3.	NAND with 2 Inputs and 3 Inputs	3 <sup>rd</sup>	2
4.	NOR with 2 Inputs and 3 Inputs	4 <sup>th</sup>	2
5.	XOR and XNOR	5 <sup>th</sup>	2
6.	XOR by using NAND gates	6 <sup>th</sup>	2
7.	XOR by using NOR gates	7 <sup>th</sup>	2
8.	Decoder	8 <sup>th</sup>	2
9.	Decoder with 7 segments	9 <sup>th</sup>	2
10.	Encoder	10 <sup>th</sup>	2
11.	Multiplexer	11 <sup>th</sup>	2
12.	Demultiplexer	12 <sup>th</sup>	2
13.	Review	13 <sup>th</sup>	
14.	Term Project Presentation	14 <sup>th</sup>	2

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas





15.	Lab Exam	15 <sup>th</sup>	2
<b>Number of Weeks /and Units Per Semester</b>		<b>15</b>	<b>30</b>

<b>VI. Teaching strategies of the course:</b>	
<ul style="list-style-type: none"> <li>- Active Lectures,</li> <li>- Hands on Lab Work,</li> <li>- Computer-based Lab Work,</li> <li>- Class Discussion</li> <li>- Problem Solving</li> <li>- Projects &amp; Presentations</li> </ul>	

<b>VII. Assignments &amp; Reports:</b>			
No	Assignments	Week Due	Mark
1.	Number Systems and their Arithmetic	3 <sup>rd</sup> & 4 <sup>th</sup>	3
2.	Boolean Algebra & K-Map Simplifications with lab Report.	6 <sup>th</sup> & 9 <sup>th</sup>	6
3.	Combinational Logic Circuits Design (Adders, Sub, Multipliers, Divisions, Comparators, MUXs. & Decoders) with lab Reports.	10 <sup>th</sup> to 13 <sup>th</sup>	6
<b>Total Marks</b>			<b>15</b>

<b>VIII. Schedule of Assessment Tasks for Students During the Semester:</b>				
No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment
1.	Assignments & Reports	3 <sup>rd</sup> to 13 <sup>th</sup>	15	10%
2.	Quizzes	5 <sup>th</sup> , 10 <sup>th</sup> & 14 <sup>th</sup>	10	6.67%
3.	Midterm Exam (Theory)	8 <sup>th</sup>	20	13.33%

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



4.	Final Lab. Exam (including Course Project Evaluation)	14 <sup>th</sup> & 15 <sup>th</sup>	30	20%
5.	Final Exam (Theory)	16 <sup>th</sup>	75	50%
<b>Total Marks / Percentage</b>			<b>150</b>	<b>100%</b>

<b>IX. Learning Resources:</b>	
<ul style="list-style-type: none"> <li>Written in the following order: ( Author - Year of publication – Title – Edition – Place of publication – Publisher).</li> </ul>	
<b>1- Required Textbook(s) ( maximum two ).</b>	
	1 -Thomas L. Floyd, 2009, Digital Fundamentals, 10 <sup>th</sup> Edition, Pearson Education International 2- Ronald J. Tocci, Neal S.Widmer, Gregory L. Moss, 2007, Digital Systems : Principles and Applications, 10 <sup>th</sup> Edition,. Pearson Prentice Hall
<b>2- Essential References.</b>	
	1-Douglas L. Perry, 2002, VHDL Programming by Example, 4 <sup>th</sup> Edition, McGraw-H 2 -M. M. Mano, M. D. Ciletti, 2007, Digital Design, 4 <sup>th</sup> Edition, Prentice-Hall
<b>3- Electronic Materials and Web Sites etc.</b>	
	1-Faculty Electronic Library

<b>X. Course Policies:</b>	
<b>1.</b>	<b>Class Attendance:</b> -A student should attend not less than 75 % of total hours of the subject; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring <b>an approved</b> statement from university Clinic
<b>2.</b>	<b>Tardy:</b> - For late in attending the class, the student will be initially notified. If he repeated lateness in attending class he will be considered as absent.
<b>3.</b>	<b>Exam Attendance/Punctuality:</b>

Prepared by	Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad
-------------	--	---	--	---

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas



	- A student should attend the exam on time. He is Permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam.
4.	<b>Assignments &amp; Projects:</b> - The assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time.
5.	<b>Cheating:</b> - For cheating in exam, a student will be considered as <b>failure</b> . In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.
6.	<b>Plagiarism:</b> Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee <b>proved</b> a plagiarism of a student, he will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university.
7.	<b>Other policies:</b> - Mobile phones are not allowed to use during a class lecture. It must be closed, otherwise the student will be asked to leave the lecture room - Mobile phones are not allowed in class during the examination. Lecture notes and assignments my given directly to students using soft or hard copy

Prepared by      Head of Department      Quality Assurance Unit      Dean of the Faculty      Academic Development  
 Asst. Prof. Dr. Adel      Assoc. Prof. Dr.      Prof. Dr. Mohammed      Center & Quality Assurance  
 Ahmed Al-Shakiri      Mohammad Algorafi      AL-Bukhaiti      Assoc. Prof. Dr. Huda Al-Emad

Rector of Sana'a University  
 Prof. Dr. Al-Qassim Mohammed Abbas