29.Course Specification of Electronics (2)

I.Course Identification and General Information:

.1	Course Title:	Electronics (2).				
.2	Course Code & Number:	MT202.				
.3	Credit hours:	C.H				TOTAL CR. HRS.
		Th.	Seminar	Pr	Tu.	
		2	-	2	2	4
.4	Study level/ semester at which this course is offered:	Third Year - First Semester.				
.5	Pre –requisite (if any):	Electronics (1) and Logic System Design.				
6.	Co –requisite (if any):	None.				
.7	Program (s) in which the course is offered:	Mechatronics Engineering Program.				
.8	Language of teaching the course:	English Language.				
.9	Location of teaching the course:	Mechatronics Engineering Department.				
10.	Prepared By:	Assoc. Prof. Dr. Farouk AL-Fuhaidy.				
11.	Date of Approval:					

II.Course Description:

This course is the foundation of all modern electronic devices based on digital integrated circuits, such as cellular phones, MP3 players, laptop computers, digital cameras, high definition televisions. It illustrates to students the fundamental principles, concepts, and importance of digital electronics and their applications. The course includes a basic understanding of the basic components as NMOS and CMOS inverters, MOS memory, storage circuits, adder, comparator, encoder, decoder ADC and DAC, multiplexer and de-multiplexer, and VHDL programming. The importance of this course is its development of integrated circuits which play a significant role in solving the problems of logic circuits. These integrated circuits facilitate the placement of a large number of transistors and on a single chip and gain in speed and consummation power.

III.Course Intended learning outcomes (CILOs) of the course		Referenced PILOs
a1.	Classify knowledge of basic concepts, fundamentals, characteristics, and design factors related to CMOS based integrated circuits.	A1
a2.	Depict principles and important parameters taking into consideration while designing digital integrated circuits.	A2

Head of the Department Assoc. Prof. Dr. Abdul-Malik Momin	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad	Rector of Sana'a University Prof. Dr. Al-Qassim Mohammed Abbas

b1.	Contrast digital integrated systems problems using VHDL/Verilog simulation software and FPGA hardware tool.	B1
b2.	Construct useful digital systems based on CMOS technology considering design factors and standard specifications related to modern digital electronics devices.	B5
c1.	Conduct laboratory experiments successfully to verify theoretical concepts related to digital integrated circuits.	C1
c2.	Perform electronics problems related to digital integrated systems using FPGA tools/boards and/or VHDL/Verilog simulations software.	C2
d1.	Co-operate in work as a team leader or a part of a team coherently while preparing environmental digital systems projects and share learned knowledge successfully.	D1
d2.	Review technical reports, discuss ideas, and justify results creatively through different forms to modern digital electronics technologies.	D6

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching Strategies	Assessment Strategies
a1. Classify knowledge of basic concepts, fundamentals, characteristics, and design factors related to CMOS based integrated circuits.	• Active Lectures. • Tutorials.	• Written Assessment. • Short Essays.
a2. Depict principles and important parameters taking into consideration while designing digital integrated circuits.	• Hands-on Laboratory Work.	• Practical Assessment. • Simulation.

(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching Strategies	Assessment Strategies
b1. Contrast digital integrated systems problems using VHDL/Verilog simulation software and FPGA hardware tool.	• Design Work and Project. • Case Studies.	• Practical Assessment. • Reports.

b2. Construct useful digital systems based on CMOS technology considering design factors and standard specifications related to modern digital electronics devices.	• Hands-on Laboratory Work. • Case Studies.	• Written Assessments. • Project Reports.

© **Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies:**		
Course Intended Learning Outcomes	Teaching Strategies	Assessment Strategies
c1. Conduct laboratory experiments successfully to verify theoretical concepts related to digital integrated circuits.	• Hands-on Laboratory Work. • Design Work.	• Practical Assessment. • Laboratory Reports.
c2. Perform electronics problems related to digital integrated systems using FPGA tools/boards and/or VHDL/Verilog simulations software.	• The Use of Communication and Information Technology	• Simulations such as Computer Based Learning.

(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching Strategies	Assessment Strategies
d1. Co-operate in work as a team leader or a part of a team coherently while preparing environmental digital systems projects and share learned knowledge successfully.	• Group Learning.	• Project Reports.
d2. Review technical reports, discuss ideas, and justify results creatively through different forms to modern digital electronics technologies.	• Active Lectures • Projects and Lab. Works.	• Project Reports.

IV.Course Content:

A – Theoretical Aspect:

Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	Contact Hours

1.	Course Orientation and Analog Power Amplifiers.	a1	Course Orientations, Power Amplifiers Main Properties and Characteristics, Classes of Power Amplifiers, Power efficiency, Class A and Class B Power Amplifiers	2	4
2.	Analog Feedback & Oscillators Electronics Circuits.	a1	Introduction to Feedback circuits, +ve and -ve feedback electronic circuits, and their analysis Electronic Oscillators Circuits, Mono-stable, Bi-stable, and A-stable Oscillators electronics circuits and their operations.	2	4
3.	Introduction to Digital Integrated Circuits.	a1,a2,b1,c2	Introduction to Digital Integrated Circuits (ICs), history and technologies, software, hardware tools, new trends, design factors, and applications.	1	2
4.	NMOS Inverters based Technology.	a1,a2,b2	History of NMOS ICs, NMOS transistors review, NMOS Inverters types, NMOS with Resistive Load, NMOS with E-MOS Load, and NMOS with D-MOS Load, electronics circuits, I/O equations, characteristics operations as a switch (inverter), VTC curves, Switching regions and times, Low-High Output voltages, Design factors effects, Inverters Sizes, Critical(Transition(s)- Voltages), VTC curves Comparison for each type of NMOS Inverters	2	4
5.	Mid-Term Exam.	a1,a2,b2	The First Four Chapters.	1	2
6.	CMOS Inverter based Technology.	a1,a2,b2	History of CMOS ICs, CMOS transistors Construction, Features & Characteristics, Operations, electronics circuits, I/O equations, illustration of its operations as a switch (an	2	4

			inverter), VTC curves, Switching regions and times, Low-High Output voltages, Aspect Ratio factor effect, Inverters Sizes, Critical (Transitions-Voltages), Noise Margin Region illustration and its equations derivation, Power Dissipation formula derivation, Propagation Delays Times derivations, comparison with NMOS Inverters NAND and NOR gates based NMOS and CMOS inverters, their operations and effects on Low-output voltage in case of NMOS-based gates and aspect ratio consideration in case of CMOS-based gates. Transmission Gates, NMOS, PMOS, and CMOS TGs constructions and operations.		
7.	Combinational Logic Circuits-based CMOS Technology and VHDL Programming.	a1, a2, b1, b2, c2	Introduction to VHDL Simulation Software, System Design Classifications, up/down and Vice-versa design terminology, structural and behavioral (Architecture) design and simulation using VHDL. Transistor-Level Design Principles and Techniques based CMOS technology, structural design, Demorgan Technique, AOI & OAI Methods, Mirror Methods, and Dynamic Implementation Method, to basic combinational logic gates & functions, multiplexers, and decoders. Digital Adders, Half-Adder and Full-Adder review and construction in transistor level based CMOS Technology	2	4

			considering different carry propagation implementation techniques like Look ahead Adder, Manchester Technique, etc. Comparator combinational Logic circuits implementation to 4-bit Magnitude Comparator and 8-bit or 16-bit word comparators.		
8.	Memory Elements-based CMOS Technology Digital Circuits .	a1, a2, b1, b2, c2	Introduction to Memory, Memory Types, Static and Dynamic Memories, RAM & ROM , Basic Building Elements, Latches and Flip-Flops Review, timing, design and implementation in transistor level based on CMOS technology and VHDL Simulation and Programming. Counters and Shift Registers implementation in Transistor Level using CMOS Technology.	2	4
9.	ADC and DAC Circuits.	a1, a2, b2	Analog-to-digital conversion circuits, Flash adder Digital-to-analog conversion electronics circuits, Ladder and R-2R Circuits.	1	2
10.	Final Exam.	a1, a2, b1, b2, c2	All the Chapters.	1	2
Number of Weeks /and Units Per Semester				**16**	**32**

B - Tutorial Aspect:

Order	Tasks/ Experiments	Number of Weeks	Contact Hours	Learning Outcomes
1.	Power Amplifiers Types, Class A and Class B Operations and Power Efficiency with Examples.	1	2	a1, a2
2.	Feedback (+ve & -ve) and Oscillators (Mono, Bi, and A stable)	1	2	a1, a2

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3.	Digital electronics: Ideal logic gates Logic levels definitions and noise margins gates Dynamic response of logic gates Logic voltage levels Noise margins Logic gate design goals Dynamic response of logic gates Rise and fall times Propagation delay Power delay product	1	2	a1, a2, b2
4.	NMOS logic design: NMOS inverter with resistive load Design of the W/L ratio of Ms Load resistor design Load-line visualization On-Resistance of the switching device Noise margin analysis Calculation of the V_{IL} and V_{OH} Calculation of Power Dissipation.	1	2	a1, a2, b2, d1, d2
5.	NMOS logic design: Load resistors problems Transistor alternatives to the load resistor Static design of the NMOS saturated load inverter, Calculation of V_H Calculation of (W/L) Noise margins analysis NMOS inverter with a linear load device (E-MOS Load) NMOS inverter with a depletion-mode (D-MOS) load Design of the W/L ratio of M_L Design of the W/L ratio of M_S Noise margins for the inverter with depletion-mode load.	1	2	a1, a2, b2, d1, d2
6.	NMOS gates and power dissipation, NMOS NAND and NOR gates NAND gates Complex NMOS logic design Selection between the two designs Static power dissipation Dynamic power dissipation Power scaling in NMOS logic gates, PMOS.	1	2	a1, a2, b2, d1, d2
7.	Complementary MOS (CMOS) logic design CMOS inverter technology CMOS inverter layout	1	2	a1, a2, b2, d1, d2

	Static characteristics of the CMOS inverter CMOS voltage transfer characteristics Noise margins for CMOS inverter.			
8.	Dynamic behavior of the CMOS inverter, Propagation delay estimate Rise and fall times Delay cascade inverters Power dissipation and power delay product in CMOS Static power dissipation Dynamic power dissipation Power delay product.	1	2	a1, a2, b2, d1, d2
9.	CMOS gates, CMOS NOR and NAND gates CMOS NOR gate CMOS NAND gates Design of complex gates in CMOS Minimum size gate design and performance.	1	2	a1, a2, b2, d1, d2
10.	Combinational Circuits: Digital adder, Half adder, Truth Table, construction, full adder, Truth Table, construction, multiple-bit adder, carry look-ahead adders. The digital comparator, type of digital comparator: comparator truth tables, truth table, 4-bit Magnitude comparator, 8-bit word comparator. Encoders and Decoders. Multiplexers and De-Multiplexers.	2	4	a1, a2, b2, c2, d1, d2
11.	Sequential Logic Circuits, Latches and Flip-Flops, Counters and Registers, Memories, Static and Dynamic, PLD RAMs types.	2	4	a1, a2, b2, c2, d1, d2
12.	Arithmetic & Logic Units Design and implementation.	1	2	a1, a2, b2, c2, d1, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

C - Practical Aspect:

Order	Tasks/ Experiments	Number of Weeks	Contact Hours	Learning Outcomes
1.	Orientation (Course Syllabus and Regulations) Laboratory Equipment and VHDL Simulation Software Installation and Familiarization.	1	2	a1, a2, b1, c1, d1
2.	Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Simulation and Practical Operation Verification.	1	2	a1, a2, b1, c1, d1

3.	N-MOSFET Gates Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	1	2	a1, a2, b1, c1, d1, d2
4.	CMOS Inverter and Logic Gates.	1	2	a1, a2, b1, c1, c2, d1
5.	Adder, Comparator Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	1	2	a1, a2, b1, b2, c1, c2 d1, d2
6.	Encoder and Decoder Simulations using VHDL/Verilog and Implantation on FPGA (if Possible in Lab).	1	2	a1, a2, b1, b2, c1, c2 d1, d2
7.	Multiplexer /De-multiplexer Simulations using VHDL/Verilog and Implantation on FPGA (if Possible in Lab).	1	2	a1, a2, b1, b2, c1, c2 d1, d2
8.	Latches and Flip-Flops Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	2	4	a1, a2, b1, b2, c1, c2 d1, d2
9.	Sequential, arithmetic, and Logic Units Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	2	4	a1, a2, b1, b2, c1, c2 d1, d2
10.	Projects Presentations.	2	4	a1, a2, b1, b2, c1, c2 d1, d2
11.	Final Practical Exam.	1	2	a1, a2, b1, b2, c1, c2, d1, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

V.Teaching strategies of the course:

- Active Lectures.
- Discussions.
- Laboratory Hands-on Work.
- Tutorials.
- Simulations.
- Office Hours.
- Work Groups.
- Projects and Report Presentations.

VI.Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	Power Amplifiers.	a1, a2	1st &2nd	1
2.	Feedback & Oscillators.	a1, a2	3trd & 4th	1
3.	NMOS Inverters.	a1, a2, b2, d1, d2	4th to 7th	1
4.	CMOS Inverter.	a1, a2, b2, d1, d2	8th & 10th	1
5.	Combinational Circuits based CMOS.	a1, a2, b1, b2, c2, d1, d2	11th & 12th	2
6.	Sequential Circuits based CMOS.	a1, a2, b1, b2, c2, d1, d2	13th	2
7.	Memory.	a1, a2, b1, b2, c2, d1, d2	14th	1
8.	ADC &DAC.	a1,a2, b2	15th	1
Total				**10**

VII.Schedule of Assessment Tasks for Students During the Semester:

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & HomeWorks.	1st to 15th	24	12%	a1, a2, b1, b2, c2, d1, d2
2.	Lab. Work and Experiments Reports.	4th to 13th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
3.	Practical Term-Project and Presentation.	3rd to 14th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
4.	Mid-Term Exam (Theoretically).	8th	16	8%	a1, a2, b2
5.	Final Term Exam (Practically).	14th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
6.	Final Term Exam (Theoretically).	16th	100	50%	a1, a2, b1, b2, c2
Total Assessments Mark/Percentage			**200**	**100%**	

VIII.Learning Resources:

- Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two).

Head of the Department	Quality Assurance Unit	Dean of the Faculty	Academic Development Center & Quality Assurance	Rector of Sana'a University
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1. John P. Uyemura, " Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc. ISBN 0-471-12704-3
2. Richard C. Jaeger and Travis N. Blalock, 2011, Microelectronic – 1 NIC circuit Design – 4/Edition – McGraw Hill Companies, USA – New York.
3. William Kleitz, 2008, Digital Electronics, a Practical Approach – Eighth Edition – PEARSON, Prentice Hall, USA.
4. M. Morris Mano & Michael D. Ciletti , 2013, Digital Design – PEARSON.

2- Essential References.

1. Raj Kamal, 2006, "Digital Principles and Design" - Pearson Education.
2. Kumar, Virender , 2009, "Digital Electronics: Theory and Experiment" – ISBN : 978-81-224-1346-5.

3- Electronic Materials and Web Sites *etc*.

1. http://www.ocw.mit.edu/courses.
2. www.ti.com/
3. http://www.motorola.com/us/consumers/home
4. http://pengchengcapacitor.en.made-in-china.com/
5. Lectures prepared by the lecturer

Reviewed By	Vice Dean for Academic Affairs and Post Graduate Studies: Asst. Prof. Dr. Tarek A. Barakat. President of Quality Assurance Unit: Assoc. Prof. Dr. Mohammed Algorafi. Head of Mechatronics Engineering Department: Assoc. Prof. Dr. Abdul-Malik Momin.
	Deputy Rector for Academic Affairs Assoc. Prof. Dr. Ibrahim AlMutaa. Assoc. Prof. Dr. Ahmed Mujahed and Asst. Prof. Dr. Munaser Alsubari.

IX.Course Policies:	
1.	**Class Attendance:** attendance according to rules and regulations The students should have more than 75 % of of the Faculty.
2.	**Tardy:** The students should respect the timing of attending the lectures. They should attend within 10 minutes from starting of the lecture.
3.	**Exam Attendance/Punctuality:** The student should attend the exam on time. The punctuality should be implemented according to rules and regulations of the faculty for mid-term exam and final exam.
4.	**Assignments & Projects:** The assignment is given to the students after each chapter, the student has to submit all the assignments for checking on time.
5.	**Cheating:** If any cheating occurred during the examination, the student is not allowed to continue and he has to face the examination committee for enquiries .
6.	**Plagiarism:** The student will be terminated from the Faculty, if one student attend the exam on another behalf according to the policy, rules and regulations of the university.
7.	**Other Policies:** All the teaching materials should be kept out the examination hall. The mobile phone is not allowed. There should be a respect between the student and his teacher.

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Template for Course Plan Electronics (2)

I.Information about Faculty Member Responsible for the Course:							
Name of Faculty Member	Assoc. Prof. Dr Farouk AL-Fuahidy	**Office Hours**					
Location& Telephone No.	+967-777909815	**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail	farouqakh@gmail.com						

II.Course Identification and General Information:						
1.	Course Title:	Electronics (2).				
2.	Course Number & Code:	MT 202.				
3.	Credit hours:	C.H				Total Cr. Hrs.
		Th.	Seminar	Pr.	Tu.	
		2	-	2	2	4
4.	Study level/year at which this course is offered:	Third Year- First Semester.				
5.	Pre –requisite (if any):	Electronics (1) and Logic System Design.				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered	Mechatronics Engineering Program.				
8.	Language of teaching the course:	English Language.				
9.	System of Study:	Semesters.				
10.	Mode of delivery:	Lectures, Tutorials and Lab.Work..				
11.	Location of teaching the course:	Mechatronics Engineering Department.				

III.Course Description:

This course is the foundation of all modern electronic devices based on digital integrated circuits, such as cellular phones, MP3 players, laptop computers, digital cameras, high definition televisions. It illustrates to students the fundamental principles, concepts, and importance of digital electronics and their applications. The course includes a basic understanding of the basic components as NMOS and CMOS inverters, MOS memory, storage circuits, adder, comparator, encoder, decoder ADC and DAC, multiplexer and de-multiplexer, and VHDL programming. The importance of this course is its development of integrated circuits which play a significant role in solving the problems of logic circuits. These integrated circuits facilitate the placement of large number of transistors and on a single chip and gain in speed and consummation power.

IV.Course Intended learning outcomes (CILOs) of the course		Referenced PILOs
a1.	Classify knowledge of basic concepts, fundamentals, characteristics, and design factors related to CMOS based integrated circuits.	A1
a2.	Depict principles and important parameters taking into consideration while designing digital integrated circuits.	A2
b1.	Contrast digital integrated systems problems using VHDL/Verilog simulation software and FPGA hardware tool.	B1
b2.	Construct useful digital systems based on CMOS technology considering design factors and standard specifications related to modern digital electronics devices.	B5
c1.	Conduct laboratory experiments successfully to verify theoretical concepts related to digital integrated circuits.	C1
c2.	Perform electronics problems related to digital integrated systems using FPGA tools/boards and/or VHDL/Verilog simulations software.	C2
d1.	Co-operate in work as a team leader or a part of a team coherently while preparing environmental digital systems projects and share learned knowledge successfully.	D1
d2.	Review technical reports, discuss ideas, and justify results creatively through different forms to modern digital electronics technologies.	D6

V.Course Content:

A – Theoretical Aspect:

Order	Units/Topics List	Sub Topics List	Number of Weeks	Contact Hours
1.	Course Orientation and Analog Power Amplifiers.	Course Orientations, Power Amplifiers Main Properties and Characteristics, Classes of Power Amplifiers, Power efficiency, Class A and Class B Power Amplifiers	1,2	4
2.	Analog Feedback & Oscillators Electronics Circuits.	Introduction to Feedback circuits, +ve and -ve feedback electronic circuits, and their analysis Electronic Oscillators Circuits, Mono-stable, Bi-stable, and A-stable Oscillators electronics circuits and their operations.	3,4	4

3.	Introduction to Digital Integrated Circuits.	Introduction to Digital Integrated Circuits (ICs), history and technologies, software, hardware tools, new trends, design factors, and applications.	5	2
4.	NMOS Inverters based Technology.	History of NMOS ICs, NMOS transistors review, NMOS Inverters types, NMOS with Resistive Load, NMOS with E-MOS Load, and NMOS with D-MOS Load, electronics circuits, I/O equations, characteristics operations as a switch (inverter), VTC curves, Switching regions and times, Low-High Output voltages, Design factors effects, Inverters Sizes, Critical(Transition(s)- Voltages), VTC curves Comparison for each type of NMOS Inverters	6,7	4
5.	Mid-Term Exam.	The First Four Chapters.	8	2
6.	CMOS Inverter based Technology.	History of CMOS ICs, CMOS transistors Construction, Features & Characteristics, Operations, electronics circuits, I/O equations, illustration of its operations as a switch (an inverter), VTC curves, Switching regions and times, Low-High Output voltages, Aspect Ratio factor effect, Inverters Sizes, Critical (Transitions-Voltages), Noise Margin Region illustration and its equations derivation, Power Dissipation formula derivation, Propagation Delays Times derivations, comparison with NMOS Inverters NAND and NOR gates based NMOS and CMOS inverters, their operations and effects on Low-output voltage in case of NMOS-based gates and aspect ratio consideration in case of CMOS-based gates. Transmission Gates, NMOS, PMOS, and CMOS TGs constructions and operations.	9,10	4

7.	Combinational Logic Circuits-based CMOS Technology and VHDL Programming.	Introduction to VHDL Simulation Software, System Design Classifications, up/down and Vice-versa design terminology, structural and behavioral (Architecture) design and simulation using VHDL. Transistor-Level Design Principles and Techniques based CMOS technology, structural design, Demorgan Technique, AOI & OAI Methods, Mirror Methods, and Dynamic Implementation Method, to basic combinational logic gates & functions, multiplexers, and decoders. Digital Adders, Half-Adder and Full-Adder review and construction in transistor level based CMOS Technology considering different carry propagation implementation techniques like Look ahead Adder, Manchester Technique, …etc. Comparator combinational Logic circuits implementation to 4-bit Magnitude Comparator and 8-bit or 16-bit word comparators.	11,12	4
8.	Memory Elements-based CMOS Technology Digital Circuits .	Introduction to Memory, Memory Types, Static and Dynamic Memories, RAM & ROM , Basic Building Elements, Latches and Flip-Flops Review, timing, design and implementation in transistor level based on CMOS technology and VHDL Simulation and Programming. Counters and Shift Registers implementation in Transistor Level using CMOS Technology.	13,14	4
9.	ADC and DAC Circuits.	Analog-to-digital conversion circuits, Flash adder Digital-to-analog conversion electronics circuits, Ladder and R-2R Circuits.	15	2
10.	Final Exam.	All the Chapters.	16	2
Number of Weeks /and Units Per Semester			**16**	**32**

B - Tutorial Aspect:				
Order	**Tasks/ Experiments**	**Number of Weeks**	**Contact Hours**	**Learning Outcomes**
1.	Power Amplifiers Types, Class A and Class B Operations and Power Efficiency with Examples.	1	2	a1, a2
2.	Feedback (+ve & -ve) and Oscillators (Mono, Bi, and A stable)	2	2	a1, a2
3.	Digital electronics: Ideal logic gates Logic levels definitions and noise margins gates Dynamic response of logic gates Logic voltage levels Noise margins Logic gate design goals Dynamic response of logic gates Rise and fall times Propagation delay Power delay product	3	2	a1, a2, b2
4.	NMOS logic design: NMOS inverter with resistive load Design of the W/L ratio of Ms Load resistor design Load-line visualization On-Resistance of the switching device Noise margin analysis Calculation of the V_{IL} and V_{OH} Calculation of Power Dissipation.	4	2	a1, a2, b2, d1, d2
5.	NMOS logic design: Load resistors problems Transistor alternatives to the load resistor Static design of the NMOS saturated load inverter, Calculation of V_H Calculation of (W/L) Noise margins analysis NMOS inverter with a linear load device (E-MOS Load) NMOS inverter with a depletion-mode (D-MOS) load Design of the W/L ratio of M_L Design of the W/L ratio of M_S Noise margins for the inverter with depletion-mode load.	5	2	a1, a2, b2, d1, d2
6.	NMOS gates and power dissipation, NMOS NAND and NOR gates NAND gates Complex NMOS logic design Selection between the two designs Static power	6	2	a1, a2, b2, d1, d2

	dissipation Dynamic power dissipation Power scaling in NMOS logic gates, PMOS.			
7.	Complementary MOS (CMOS) logic design CMOS inverter technology CMOS inverter layout Static characteristics of the CMOS inverter CMOS voltage transfer characteristics Noise margins for CMOS inverter.	7	2	a1, a2, b2, d1, d2
8.	Dynamic behavior of the CMOS inverter, Propagation delay estimate Rise and fall times Delay cascade inverters Power dissipation and power delay product in CMOS Static power dissipation Dynamic power dissipation Power delay product.	8	2	a1, a2, b2, d1, d2
9.	CMOS gates, CMOS NOR and NAND gates CMOS NOR gate CMOS NAND gates Design of complex gates in CMOS Minimum size gate design and performance.	9	2	a1, a2, b2, d1, d2
10.	Combinational Circuits: Digital adder, Half adder, Truth Table, construction, full adder, Truth Table, construction, multiple-bit adder, carry look-ahead adders. The digital comparator, type of digital comparator: comparator truth tables, truth table, 4-bit Magnitude comparator, 8-bit word comparator. Encoders and Decoders. Multiplexers and De-Multiplexers.	10,11	4	a1, a2, b2, c2, d1, d2
11.	Sequential Logic Circuits, Latches and Flip-Flops, Counters and Registers, Memories, Static and Dynamic, PLD RAMs types.	12,13	4	a1, a2, b2, c2, d1, d2
12.	Arithmetic & Logic Units Design and implementation.	14	2	a1, a2, b2, c2, d1, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

C - Practical Aspect:

Order	Tasks/ Experiments	Number of Weeks	Contact Hours	Learning Outcomes
1.	Orientation (Course Syllabus and Regulations)	1	2	a1, a2, b1, c1, d1

	Laboratory Equipment and VHDL Simulation Software Installation and Familiarization.			
2.	Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Simulation and Practical Operation Verification.	2	2	a1, a2, b1, c1, d1
3.	N-MOSFET Gates Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	3	2	a1, a2, b1, c1, d1, d2
4.	CMOS Inverter and Logic Gates.	4	2	a1, a2, b1, c1, c2, d1
5.	Adder, Comparator Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	5	2	a1, a2, b1, b2, c1, c2 d1, d2
6.	Encoder and Decoder Simulations using VHDL/Verilog and Implantation on FPGA (if Possible in Lab).	6	2	a1, a2, b1, b2, c1, c2 d1, d2
7.	Multiplexer /De-multiplexer Simulations using VHDL/Verilog and Implantation on FPGA (if Possible in Lab).	7	2	a1, a2, b1, b2, c1, c2 d1, d2
8.	Latches and Flip-Flops Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	8,9	4	a1, a2, b1, b2, c1, c2 d1, d2
9.	Sequential, arithmetic, and Logic Units Simulations using VHDL/Verilog and Implementation on FPGA (if Possible in Lab).	10,11	4	a1, a2, b1, b2, c1, c2 d1, d2
10.	Projects Presentations.	12,13	4	a1, a2, b1, b2, c1, c2 d1, d2
11.	Final Practical Exam.	14	2	a1, a2, b1, b2, c1, c2, d1, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

VI.Teaching strategies of the course:

- Active Lectures.
- Discussions.
- Laboratory Hands-on Work.

- Tutorials.
- Simulations.
- Office Hours.
- Work Groups.
- Projects and Report Presentations.

VII.Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	Power Amplifiers.	a1, a2	1st &2nd	1
2.	Feedback & Oscillators.	a1, a2	3trd & 4th	1
3.	NMOS Inverters.	a1, a2, b2, d1, d2	4th to 7th	1
4.	CMOS Inverter.	a1, a2, b2, d1, d2	8th & 10th	1
5.	Combinational Circuits based CMOS.	a1, a2, b1, b2, c2, d1, d2	11th & 12th	2
6.	Sequential Circuits based CMOS.	a1, a2, b1, b2, c2, d1, d2	13th	2
7.	Memory.	a1, a2, b1, b2, c2, d1, d2	14th	1
8.	ADC &DAC.	a1,a2, b2	15th	1
	Total			**10**

VIII.Schedule of Assessment Tasks for Students During the Semester:

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & HomeWorks.	1st to 15th	24	12%	a1, a2, b1, b2, c2, d1, d2
2.	Lab. Work and Experiments Reports.	4th to 13th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
3.	Practical Term-Project and Presentation.	3rd to 14th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
4.	Mid-Term Exam (Theoretically).	8th	16	8%	a1, a2, b2
5.	Final Term Exam (Practically).	14th	20	10%	a1, a2, b1, b2, c1, c2, d1, d2
6.	Final Term Exam (Theoretically).	16th	100	50%	a1, a2, b1, b2, c2

Total Assessments Mark/Percentage	**200**	**100%**	

IX.Learning Resources:

- Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two).

1. John P. Uyemura, " Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc. ISBN 0-471-12704-3
2. Richard C. Jaeger and Travis N. Blalock, 2011, Microelectronic – 1 NIC circuit Design – 4/Edition – McGraw Hill Companies, USA – New York.
3. William Kleitz, 2008, Digital Electronics, a Practical Approach – Eighth Edition – PEARSON, Prentice Hall, USA.
4. M. Morris Mano & Michael D. Ciletti , 2013, Digital Design – PEARSON.

2- Essential References.

1. Raj Kamal, 2006, "Digital Principles and Design" - Pearson Education.
2. Kumar, Virender , 2009, "Digital Electronics: Theory and Experiment" – ISBN : 978-81-224-1346-5.

3- Electronic Materials and Web Sites *etc*.

1. http://www.ocw.mit.edu/courses.
2. www.ti.com/
3. http://www.motorola.com/us/consumers/home
4. http://pengchengcapacitor.en.made-in-china.com/
5. Lectures prepared by the lecturer

X.Course Policies:	
1.	**Class Attendance:** attendance according to rules and regulations of The students should have more than 75 % of the Faculty.
2.	**Tardy:** The students should respect the timing of attending the lectures. They should attend within 10 minutes from starting of the lecture.
3.	**Exam Attendance/Punctuality:** The student should attend the exam on time. The punctuality should be implemented according to rules and regulations of the faculty for mid-term exam and final exam.
4.	**Assignments & Projects:** The assignment is given to the students after each chapter, the student has to submit all the assignments for checking on time.
5.	**Cheating:** If any cheating occurred during the examination, the student is not allowed to continue and he has to face the examination committee for enquiries.
6.	**Plagiarism:** The student will be terminated from the Faculty, if one student attend the exam on another behalf according to the policy, rules and regulations of the university.
7.	**Other Policies:** All the teaching materials should be kept out the examination hall. The mobile phone is not allowed. There should be a respect between the student and his teacher.