Sana'a University
Faculty of Engineering
Electrical Engineering Department
B.Sc. of Computer and Control Engineering

34. Course Plan of Digital Electronic Circuits

I. Information about Faculty Member Responsible for the Course

Name of Faculty Member	Prof. Abdul Raqib Abdo Asaad	**Office Hours**					
Location& Telephone No.		**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail							

II. Course Identification and General Information

1.	Course Title:	Digital Electronic Circuits				
2.	Course Number & Code:	CCE213				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	-	2	-	3
4.	Study level/year at which this course is offered:	Third Year/ Second Semester				
5.	Pre –requisite (if any):	Logic Circuit (I), Logic Circuit (II), Electronics (I)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered	B.Sc. of Computer and Control Engineering				
8.	Language of teaching the course:	Arabic & English				
9.	System of Study:	Semesters				
10.	Mode of delivery:	Lecture				
11.	Location of teaching the course:	Class Room (Faculty of Engineering)				

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III. Course Description

This course aims to provide students with the basic fundamentals and concepts required to the design and implementation of digital integrated circuits. Digital ICs have many different applications in new technologies and smart devices such as mobiles, MP3 devices, digital computers, GPUs and controllers. Course topics includes an introduction to digital ICs analysis and design parameters, DL, DTL, NMOS & CMOS inverters and ICs technologies, and the construction of Combinational and Sequential logic circuits in transistor level as well as their simulation using VHDL. This course is supported with lab sessions and course project work to develop students' skills to the design and simulation of ICs.

IV. Course Aims

This course aims to:

1. Introduce the internal operation of the digital electronic circuits.
2. Analyze digital electronic circuits for DL, DTL, DCTL, and RTL logic gates.
3. Analyze digital electronic circuits for TTL, ECL, MOS, AND CMOS logic gates.
4. Design digital integrated circuits.

V. Intended learning outcomes (ILOs) of the course:

1. Explain the internal operation of the digital electronic circuits as well as their design factors and applications to the field of computer engineering and control.
2. Define principles and simulation and programming tools of digital electronics design.
3. Identify the transistor and logic levels and logic states at the input and output of logic gates, and the characteristics of operation.
4. Analyze digital electronic circuits for DL, DTL, DCTL, RTL, TTL, ECL, MOS, AND CMOS technologies.
5. Design different families of digital electronic circuits and digital integrated circuits.
6. Use simulation programs to design digital electronic circuits then compare the simulation results with the theoretical specifications.
7. Perform specific tasks individually and work in a group to solve specific problems.

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8.	Present his information clearly using presentation skills, satisfy the audience, by following the writing standards to achieve technical reports.

VI. Course Content

A – Theoretical Aspect

Order	Units/Topics List	Sub Topics List	Number of Weeks	Contact hours
1.	Introduction to Integrated circuit devices and modeling	▪ Introduction to ICs, Design Principles and terminologies and ICs Technologies, ▪ logic gates basics (DL, DTL, DTL, RTL)	1st ,2nd	4
2.	NMOS Inverter Technology	▪ NMOS inverters (NMOS with Resistive Load, Enhancement Load and Depletion Load), I/O characteristic Curve, Design Factors effect and Comparison, ▪ NAND & NOR gates based NMOS and their Characteristics ▪ Examples	3rd ,4th ,5th	6
3.	CMOS Inverter Technology	▪ CMOS Structure and (PMOS & PMOS) Operation, ▪ CMOS Inverter: I/O Characteristic Curve, Switching, Propagation Delay and Noise Margin, ▪ NMOS, PMOS and CMOS Transmission Gates Operations,	6th ,7th	4

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		▪ NOR & NAND Gates based on CMOS and their I/O Characteristics		
4.	Midterm Exam	▪ ALL Previous Topics	8th	2
5.	Design of Combinational Logic Circuits based on CMOS Technology	▪ Adders/Subtractors ▪ Multiplexers ▪ Decoders, ▪ ALU design based on CMOS.	9th ,10th	4
6.	Design of Sequential Logic Circuits based on CMOS Technology	▪ Latches & Flip Flops, operation characteristics and different delay times, FFs Construction based CMOS, ▪ Registers and Barrel Shift Registers construction using CMOS and TGs.	11th ,12th	4
7.	Analog to Digital and Digital to Analog Electronics Circuits	▪ Ladder ADC Circuit ▪ R-2R ADC Circuit ▪ Ramp DAC Circuit ▪ Successive Approximation DAC Circuit	13th ,14th	4
8.	Presentations	▪ Students' presentations	15th	2
9.	Final Exam	▪ ALL Topics	16th	2
Number of Weeks /and Units Per Semester			**16**	**32**

B - Practical Aspect			
Based on VHDL and Computer Labs			
Order	**Topics List**	**Number of Weeks**	**Contact hours**

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1.	Integrated circuit devices and modeling, logic gates basics (DL, DTL, DTL, RTL)	1st ,2nd ,3rd	6
2.	Analysis and Design of basic & Standard Logic Gates based on NMOS & CMOS Inverters	4th ,5th ,6th	6
3.	Combinational Logic Circuit Design and Analysis based on NMOS and CMOS Technologies	7th ,8th ,9th	6
4.	Analyze and design of DTL, TTL, ECL, MOS (PMOS, NMOS), COMS gates, Flip-Flops, Registers and memory circuits.	10th ,11th ,12th ,13th	8
5.	Final Lab Exam	14th	2
Number of Weeks /and Units Per Semester		**14**	**28**

VII. Teaching strategies of the course

- Lectures
- Homework
- Laboratory Work
- Dialogue and discussion
- Self-learning
- Project

VIII. Assignments & Reports

No	Assignments	Aligned CILOs	Week Due	Mark
1.	Search Web, Prepare Report for ICs and Recent Technology based ICs	a1, a2, b1, b2, d1, d2	3rd	2
2.	Assignment on NMOS & CMOS Technologies	a1, a2, b1, b2, c1, d1	4th to 7th	2
3.	Combinational & Sequential Circuits Assignment	a1, a2, b1, b2, c1, c2, d1	9th to 14th	4

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4.	Lab Reports	a1, a2, b1, b2, c1, c2, d1, d2	3rd to 13th	7
Total				**15**

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IX. Schedule of Assessment Tasks for Students during the Semester

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & Reports	3rd to 14th	15	10%	a1, a2, b1, b2, c1, c2, d1, d2
2.	Quizzes	4th, 6th, and 14th	7.5	5%	a1, a2, b1, b2, c1
3.	Midterm Exam	8th	22.5	15%	a1, a2, b1, b2, c1
4.	Final Lab Exam (including Course Project Evaluation)	14th	30	20%	a1, a2, b1, b2, c1, c2, d1, d2
5.	Final Exam	16th	75	50%	a1, a2, b1, b2, c1
Total			**150**	**100%**	

X. Learning Resources

Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two)

1. Richard C. Jaeger, Travis N. Blalock (1998), Microelectronic Circuit Design, Second Edition, McGraw-Hill.
2. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic (2003), Digital Integrated Circuits: A design Perspective, Second Edition, Pearson Prentice Hall.

2- Essential References

1. Hodges, D. A. and H. G. Jackson, (1988), Analysis and Design of Digital Integrated Circuits, Second Edition. McGraw-Hill.
2. Sedra, A. S. and K. C. Smith (1990), Microelectronic Circuits. Third Edition. Saunders, Philadelphia, PA.

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	3. Glasford, G. M. (1988), Digital Electronic Circuits. Prentice-Hall, Englewood Cliffs, NJ. 4. J. R. Houser (1993), "Noise margin criteria for digital logic circuits," IEEE Trans. on Education, vol. 36, no.4. 5. J. D. Meindl and J. A. Davis (2000), "The fundamental limit on binary switching energy for terascale integration (TSI)", IEEE Journal of Solid-State Circuits, vol. 35, no. 10.
3- Electronic Materials and Web Sites etc.	

XI. Course Policies:

1.	**Class Attendance:** -A student should attend not less than 75 % of total hours of the subject; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring an approved statement from university Clinic
2.	**Tardy:** - For late in attending the class, the student will be initially notified. If he repeated lateness in attending class he will be considered as absent.
3.	**Exam Attendance/Punctuality:** - A student should attend the exam on time. He is Permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam.
4.	**Assignments & Projects:** - The assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time.
5.	**Cheating**: - For cheating in exam, a student will be considered as failure. In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.

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6.	**Plagiarism**: Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee proved a plagiarism of a student, he will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university.
7.	**Other policies:** - Mobile phones are not allowed to use during a class lecture. It must be closed, otherwise the student will be asked to leave the lecture room - Mobile phones are not allowed in class during the examination. Lecture notes and assignments my given directly to students using soft or hard copy

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