19. Course Specification of Logic Circuits

I. Course Identification and General Information:

1.	Course Title:	Logic Circuits				
2.	Course Code & Number:	CCE118				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	2	2	-	4
4.	Study level/ semester at which this course is offered:	Second Year/First Semester				
5.	Pre –requisite (if any):	Computer skills (UR003)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered:	Power Engineering and Electrical Machines				
8.	Language of teaching the course:	English				
9.	Location of teaching the course:	Faculty of Engineering				
10.	Prepared By:	Asst. Prof. Dr. Adel Al-Shogairy				
11.	Date of Approval					

II. Course Description:

This course introduces students to the digital principles with emphasis on logic design. It covers Number systems, binary arithmetic and codes, logic gates, Boolean algebra and logic simplifications, design and realization of combinational circuits, Functions of combinational circuits logic using NAND and NOR gates. Learn the principles of analysis and design of combinational logic circuits. Learn the principles of analysis and design of sequential logic circuits.

By the end of the course, students – in groups- will be asked to submit a project in which their elements are basic logic gates and combinational logic circuits learned by the course. Finally, this course provides the basic concepts required to study the Logic System Design, the Digital Electronic Circuits, and the Microprocessors & Microcontrollers courses.

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	III. Course Intended learning outcomes (CILOs) of the course	Referenced PILOs
a1	Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.	A1
a2	Acquire knowledge about a digital system, components or process to meet desired needs within realistic constraints.	A3
b1	Solve engineering problems in the area of digital logic circuit design.	B2
b2	Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.	B4
c1	Design digital logic circuits using apply knowledge of number systems, codes and Boolean algebra.	C2
c2	Use the techniques, skills, and modern engineering tools necessary for engineering practice.	C3
d1	Function on teams through digital circuit experiments and projects.	D1

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
a1. Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.	▪ Lecture ▪ Presentation	▪ Quizzes ▪ Homework ▪ Test
a2. Acquire knowledge about a digital system, components or process to meet desired needs within realistic constraints.	▪ Lecture ▪ Presentation ▪ Class Discussion	▪ Quizzes Homework ▪ Test

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(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
b1. Solve engineering problems in the area of digital logic circuit design.	▪ Lecture ▪ Presentation ▪ Class Discussion ▪ Problem Solving	▪ Quizzes ▪ Homework ▪ Written Exam.
b2. Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.	▪ Lecture ▪ Problem Solving ▪ Laboratory Work	▪ Quizzes ▪ Homework ▪ Written Exam.

© Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
c1. Design digital logic circuits using apply knowledge of number systems, codes and Boolean algebra.	▪ Lecture ▪ Presentation ▪ Class Discussion ▪ Problem Solving	▪ Quizzes ▪ Homework ▪ Written Exam.
c2. Use the techniques, skills, and modern engineering tools necessary for engineering practice.	▪ Lecture ▪ Presentation ▪ Problem Solving	▪ Quizzes ▪ Homework ▪ Written Exam.

(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
d1- Function on teams through digital circuit experiments and projects.	▪ Lecture ▪ Lab Work ▪ Class Discussion	▪ Quizzes ▪ Small Projects

IV. Course Content:

A – Theoretical Aspect:

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Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	Contact hours
1.	Introduction to Logic Circuits and its applications	a.1,a.2	• Analog and Digital Systems • Binary Digits and Logic Levels • Digital Waveforms • Timing Diagrams • Serial and Parallel Data • Basic Logic Functions • Programmable Logic • Logic CAD system (VHDL)	1	2
2.	Number systems and Codes	a.2, b.1, b.2, c.1, c.2	• Binary, Octal and Hex Number Systems • Number Systems Conversions. • BCD, Gray and Alphanumeric Codes. • Error Detection.	1	2
3.	Digital Arithmetic	a.2, b.1, b.2, c.1, c.2	• Binary addition and Subtraction. • Binary Multiplication and Division. • BCD Addition and Hex. Arithmetic	2	4
4.	Logic Gates	a.1, a.2, b.1, b.2, c.1, c.2	• Boolean Constants and Variables. • Truth Tables. • OR, AND, and NOT Operations. • Logic Algebra and Logic Implementation. • NOR and NAND Gates	2	4

5.	Boolean Algebra and Logic Simplification	a.2, b.1, b.2, c.1, c.2, d.1	• Boolean and Demorgan's Theorems. • Universality of NAND and NOR Gates. • Alternative Representations. • Labeling Logic Signals. • SOP and POS Forms. • Simplifying Logic Circuits using algebra and K-maps.	2	4
6.	Combinational Logic	a.1, b.1, b.2, c.1, c.2	• Introduction • Basic Circuits and Design Procedure. • Using NAN and NOR gates in Design. • Display Devices	2	4
7.	Combinational Circuits	b.1, b.2, c.1, c.2, d.1	• Introduction. • Arithmetic Circuits and Comparators. • Decoders, and Encoders. • Multiplexers and Demultiplexers.	2	4
8.	Combinational Logic Programming	b.1, b.2, c.1, c.2, d.1	• Introduction • Describing Logic circuits • Development Software • Description languages and Programming Languages • Implementing Logic Circuits using PLDs • VHDL Format and Syntax • Intermediate signals in VHDL • Representing Data in VHDL • Truth Tables using VHDL	2	4

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			• Decision Control Structures • Implementing Adders, Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators, Code Converters.		
Number of Weeks /and Units Per Semester				**14**	**28**

B – Tutorial Aspect:

Order	Tasks/ Experiments	Number of Weeks	Contact hours	Learning Outcomes
1.	Logic Gates 1	1	2	b.1, c.1, c.2, d.1
2.	Logic Gates 2	1	2	b.2, c.1, c.2, d.1
3.	Logic Gates 3	1	2	b.1, b.2, c.2, d.1
4.	Logic Gates 4	1	2	b.1, b.2, c.1, , d.1
5.	Logic Gates 5	1	2	b.1, b.2, c.1, c.2,
6.	Logic Gates 6	1	2	b.1, b.2, c.1, c.2, d.1
7.	Combinational Logic	2	4	, b.2, c.1, c.2, d.1
8.	Combinational Circuits	2	4	b.1, b.2, c.2, d.1
9.	Combinational Logic Programming	4	8	b.1, b.2, c.1, c.2, d.1
Number of Weeks /and Units Per Semester 14			**28**	

C - Practical Aspect:				
No.	**Tasks/ Experiments**	**No. of Weeks**	**Contact Hours**	**Learning Outcomes**
1.	Lab Equipment Orientations, Simulation Software required in the design of sequential circuits and Digital Systems	1	2	a1, c2
2.	Introduction to VHDL and FPGA	2	4	a1, c2
3.	Laches and Flip-Flops practical implementation and description of their operations and VHDL design.	2	4	c1, c2, d1
4.	Sequential Logic circuits design (Sequence Detector Circuits) using VHDL and Lap Equipment	2	4	c1, c2, d1
5.	Counter Design and Implementation	2	4	c1, c2, d1
6.	Shift Register Design	1	2	c1, c2, d1
7.	Memory Device Design, PLD and PLA Design using VHDL and FPGA	2	4	a1, c1, c2, d1
8.	Review	2	4	a1, c1, c2, d1, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

V. Teaching strategies of the course:

- Lecture
- Lab Work
- Class Discussion
- Problem Solving
- Presentation

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VI. Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	System Numbers, Binary Arithmetic, and Complements	a1	3rd	2
2.	Boolean Algebra	a1, b1	4th and 5th	2
3.	K-Map	a1, b1	6th and 7th	2
4.	Combinational Logic Circuits Design	a1, a2, b1, b2	9th to 15th	4
Total				**10**

VII. Schedule of Assessment Tasks for Students During the Semester:

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments	3nd to 15th	10	5%	a1, a2, b1, b2
2.	Quizzes	5th, 10th, and 14th	10	5%	a1, a2, b1, b2,
3.	Lab-tasks and reports	1st to 12th	20	10%	c1, c2, d1
4.	Project Presentation	14th	20	10%	a2, c1, c2, d1
5.	Practical Exam	15th	20	10%	a2,c1, c2, d1
6.	Mid-Term Exam (Theory)	7th	20	10%	a1, a2, b1, b2,
7.	Final-Term Exam (Theory)	16th	100	50%	a1, a2, b1, b2,
Total			**200**	**100%**	

VIII. Learning Resources:

- *Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).*

1- Required Textbook(s) (maximum two).

1. Thomas L. Floyd, 2009, Digital Fundamentals, 10th Edition, Pearson Education International

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	2. Ronald J. Tocci, Neal S.Widmer, Gregory L. Moss, 2007, Digital Systems : Principles and Applications, 10th Edition,. Pearson Prentice Hall
2- Essential References.	
	1. Douglas L. Perry, 2002, VHDL Programming by Example, 4th Edition, McGraw-Hill 2. M. M. Mano, M. D. Ciletti, 2007, Digital Design, 4th Edition, Prentice-Hall
3- Electronic Materials and Web Sites *etc*.	
	1. Faculty Electronic Library 2. ELectronic Lectures, PPT, Prepared by the Lecturer (if possible) 3. http://www.ocw.mit.edu/courses. 4. http://www.pearsoned.co.in/MMorrisMano/

IX. Course Policies:

1.	• **Class Attendance** A student should attend not less than 75 % of total hours of the course; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring an approved statement from university Clinic.
2.	• **Tardy** For being late in attending the class, the student will be initially notified. If he/she repeated lateness in attending class he will be considered as absent.
3.	• **Exam Attendance/Punctuality** A student should attend the exam on time. He is permitted to attend an exam half an hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam.
4.	• **Assignments and Projects** Assignments are given to the students after each chapter; students have to submit all assignments for checking on time.
5.	• **Cheating** For cheating in exam, a student will be considered as failure. In case the cheating is repeated three times during his/her study, the student will be dismissed from the Faculty.
6.	• **Plagiarism**

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	Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee proved a plagiarism of a student, he will be dismissed from the Faculty. The final dismissal of the student from the Faculty should be confirmed by the Student Council Affairs of the university.
7.	- **Other policies** - Mobile phones are not allowed to use during a class lecture. It must be closed, otherwise the student will be asked to leave the lecture room**.** - Mobile phones are not allowed in class during the examination. - Lecture notes and assignments may be given directly to students using soft and/or hard copy**.**

Reviewed By	**Vice Dean for Academic Affairs and Post Graduate Studies: Asst. Prof. Dr. Tarek A. Barakat** **President of Quality Assurance Unit: Assoc. Prof. Dr. Mohammed Algorafi** **Name of Reviewer from the Department: Assoc. Prof. Dr. Radwan Al bouthigy**
	Deputy Rector for Academic Affairs Asst. Prof. Dr. Ibrahim AlMutaa **Assoc. Prof. Dr. Ahmed Mujahed** **Asst. Prof. Dr. Munasar Alsubri**

Head of Department Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Quality Assurance Unit Assoc. Prof. Dr. Mohammad Algorafi	Dean of the Faculty Prof. Dr. Mohammed AL-Bukhaiti	Academic Development Center & Quality Assurance Assoc. Prof. Dr. Huda Al-Emad	Rector of Sana'a University Prof. Dr. Al-Qassim Mohammed Abbas

19. Template for Course Plan of Logic Circuits

I. Information about Faculty Member Responsible for the Course:

Name of Faculty Member	Asst. Prof. Dr. Adel Ahmed Al-Shogairy	**Office Hours**					
Location& Telephone No.	Electrical Eng. Dept	**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail	Ashakiri62@gmail.com		8-12		8-12		

II. Course Identification and General Information:

1.	Course Title:	Logic Circuits				
2.	Course Number & Code:	CCE118				
3.	Credit hours:	C.H				Total
		Th.	Tut.	Pr.	Tr.	
		2	2	2	-	4
4.	Study level/year at which this course is offered:	Second Year/ First Semester				
5.	Pre –requisite (if any):	Computer skills (UR003)				
6.	Co –requisite (if any):	NA				
7.	Program (s) in which the course is offered	Power Engineering and Electrical Machines				
8.	Language of teaching the course:	English				
9.	System of Study:	Regular				
10.	Mode of delivery:	Lecture				
11.	Location of teaching the course:	Class & lab				

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III. Course Description:

This course introduces students to the digital principles with emphasis on logic design. It covers Number systems, binary arithmetic and codes, logic gates, Boolean algebra and logic simplifications, design and realization of combinational circuits, Functions of combinational circuits logic using NAND and NOR gates. Learn the principles of analysis and design of combinational logic circuits. Learn the principles of analysis and design of sequential logic circuits.

By the end of the course, students – in groups- will be asked to submit a project in which their elements are basic logic gates and combinational logic circuits learned by the course. Finally, this course provides the basic concepts required to study the Logic System Design, the Digital Electronic Circuits, and the Microprocessors & Microcontrollers courses.

IV. Intended learning outcomes (ILOs) of the course:

- Brief summary of the knowledge or skill the course is intended to develop**:**

1. Define properties and characteristics of logic gates, laws and rules of Boolean Algebra, Boolean expressions, combinational circuits, and sequential circuits, K-Map, Truth Table and State Diagram.
2. Acquire knowledge about a digital system, components or process to meet desired needs within realistic constraints.
3. Solve engineering problems in the area of digital logic circuit design.
4. Analyze effectively digital logic circuit based on practical problem and implements the circuit design in lab.
5. Design digital logic circuits using apply knowledge of number systems, codes and Boolean algebra.
6. Use the techniques, skills, and modern engineering tools necessary for engineering practice.
7. Function on teams through digital circuit experiments and projects.

V. Course Content:

A – Theoretical Aspect:

Order	Units/Topics List	Sub Topics List	Number of Weeks	Contact hours
1.	Introduction to Logic Circuits and its applications	• Analog and Digital Systems • Binary Digits and Logic Levels • Digital Waveforms • Timing Diagrams • Serial and Parallel Data • Basic Logic Functions • Programmable Logic • Logic CAD system (VHDL)	1st	2
2.	Number systems and Codes	• Binary, Octal and Hex Number Systems • Number Systems Conversions. • BCD, Gray and Alphanumeric Codes. • Error Detection.	2nd	2
3.	Digital Arithmetic	• Binary addition and Subtraction. • Binary Multiplication and Division. • BCD Addition and Hex. Arithmetic	3rd ,4th	4
4.	Logic Gates	• Boolean Constants and Variables. • Truth Tables. • OR, AND, and NOT Operations. • Logic Algebra and Logic Implementation. • NOR and NAND Gates	5th ,6th	4
5.	Midterm Exam		7th	2
6.	Boolean Algebra and Logic Simplification	• Boolean and Demorgan's Theorems. • Universality of NAND and NOR Gates. • Alternative Representations. • Labeling Logic Signals. • SOP and POS Forms.	8th ,9th	4

		• Simplifying Logic Circuits using algebra and K-maps.		
7.	Combinational Logic	• Introduction • Basic Circuits and Design Procedure. • Using NAN and NOR gates in Design. • Display Devices	10^{th} ,11^{th}	4
8.	Combinational Circuits	• Introduction. • Arithmetic Circuits and Comparators. • Decoders, and Encoders. • Multiplexers and Demultiplexers.	12^{th} ,13^{th}	4
9.	Combinational Logic Programming	• Introduction • Describing Logic circuits • Development Software • Description languages and Programming Languages • Implementing Logic Circuits using PLDs • VHDL Format and Syntax • Intermediate signals in VHDL • Representing Data in VHDL • Truth Tables using VHDL • Decision Control Structures • Implementing Adders, Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators, Code Converters.	14^{th} ,15^{th}	4
10.	Final Exam		16^{th}	2
Number of Weeks /and Units Per Semester			**16**	**32**

B – Tutorial Aspect:

Order	Tasks/ Experiments	Number of Weeks	Contact hours
1.	Logic Gates 1	1^{st}	2
2.	Logic Gates 2	2^{nd}	2
3.	Logic Gates 3	3^{rd}	2

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4.	Logic Gates 4	4^{th}	2
5.	Logic Gates 5	5^{th}	2
6.	Logic Gates 6	5^{th}	2
7.	Combinational Logic	6^{th} ,7^{th}	4
8.	Combinational Circuits	8^{th} ,9^{th}	4
9.	Combinational Logic Programming	10^{th} ,11^{th} ,12^{th} ,13^{th}	8
Number of Weeks /and Units Per Semester 14			**28**

C- Practical Aspect:

No.	Tasks/ Experiments	No. of Weeks	Contact Hours
1.	Lab Equipment Orientations, Simulation Software required in the design of sequential circuits and Digital Systems	1^{st}	2
2.	Introduction to VHDL and FPGA	2^{nd} ,3^{rd}	4
3.	Laches and Flip-Flops practical implementation and description of their operations and VHDL design.	4^{th} ,5^{th}	4
4.	Sequential Logic circuits design (Sequence Detector Circuits) using VHDL and Lap Equipment	6^{th} ,7^{th}	4
5.	Counter Design and Implementation	8^{th} ,9^{th}	4
6.	Shift Register Design	10^{th}	2
7.	Memory Device Design, PLD and PLA Design using VHDL and FPGA	11^{th} ,12^{th}	4
8.	Review	13^{th}	2
9.	Project's Presentation and Final Exam (Practical)	14^{th} ,15^{th}	4
Number of Weeks /and Units Per Semester		**15**	**30**

VI. Teaching strategies of the course:

- Lecture
- Lab Work
- Class Discussion
- Problem Solving

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- Presentation

VII. Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	System Numbers, Binary Arithmetic, and Complements	a1	3rd	2
2.	Boolean Algebra	a1, b1	4th and 5th	2
3.	K-Map	a1, b1	6th and 7th	2
4.	Combinational Logic Circuits Design	a1, a2, b1, b2	9th to 15th	4
Total				**10**

VIII. Schedule of Assessment Tasks for Students During the Semester:

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment
1.	Assignments	3nd to 15th	10	5%
2.	Quizzes	5th, 10th, and 14th	10	5%
3.	Lab-tasks and reports	1st to 12th	20	10%
4.	Project Presentation	14th	20	10%
5.	Practical Exam	15th	20	10%
6.	Mid-Term Exam (Theory)	7	20	10%
7.	Final-Term Exam (Theory)	16	100	50%
Total			**200**	**100%**

IX. Learning Resources:

- *Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).*

1- Required Textbook(s) (maximum two).

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	1. Faculty Electronic Library 2. ELectronic Lectures, PPT, Prepared by the Lecturer (if possible) 3. http://www.ocw.mit.edu/courses. 4. http://www.pearsoned.co.in/MMorrisMano/

X. Course Policies:

1.	• **Class Attendance** A student should attend not less than 75 % of total hours of the course; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring an approved statement from university Clinic.
2.	• **Tardy** For being late in attending the class, the student will be initially notified. If he/she repeated lateness in attending class he will be considered as absent.
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4.	• **Assignments and Projects** Assignments are given to the students after each chapter; students have to submit all assignments for checking on time.
5.	• **Cheating** For cheating in exam, a student will be considered as failure. In case the cheating is repeated three times during his/her study, the student will be dismissed from the Faculty.
6.	• **Plagiarism**

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