Sana'a University
Faculty of Engineering
Electrical Engineering Department
B.Sc. of Computer and Control Engineering

Course Specification of Hardware Design Language

I. Course Identification and General Information

1.	Course Title:	Hardware Design Language				
2.	Course Code &Number:	CCE245				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	-	2	-	3
4.	Study level/ semester at which this course is offered:	Third Year/ First Semester				
5.	Pre –requisite (if any):	Programming Language (II), Logic Circuits (II)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered:	B.Sc. of Computer and Control Engineering				
8.	Language of teaching the course:	Arabic & English				
9.	Location of teaching the course:	Class Room (Faculty of Engineering)				
10.	Prepared By:	Prof. Abdul Raqib Abdo Asaad				
11.	Date of Approval					

II. Course Description

This course aims to provide students with basic principles, fundamentals and concepts related to the development of digital integrated circuits based on VHDL programming. Modern practices of HDLs using VHDL or Verilog languages for modeling, timing, events, etc. has raised demands and applications in industrial's digital systems evolution and development. Course topics cover review on logic gates, combinational and sequential logic circuits, FPGA, Verilog & VHDL fundamentals and programming and modeling and simulation of ICs. Based on lectures, practical & computer labs and term projects works, students will be able to develop their problem-solving, programming, modeling and simulation skills related to ICs development.

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Prof. Abdul Raqib Abdo Asaad.	Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Assoc. Prof. Dr. Mohammad Algorafi	Prof. Dr. Mohammed AL-Bukhaiti	Assoc. Prof. Dr. Huda Al-Emad

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III. Course Intended learning outcomes (CILOs) of the course		Referenced PILOs
a1	Define the principles, terminologies, and architectures of HDL and FPGA.	A1
a2	Explain the different methods of HDL applied in designing of digital circuits and systems.	A2, A3
b1	Formulate digitals system that serve complex applications.	B1, B4
b2	Analyze data of HDL simulation results for concluding the correct design.	B2, B3
c1	Implement digital circuits/systems using the training kit.	C2, C3
c2	Use HDL editor, simulation and synthesis tools for designing and implementing of digital circuits and systems.	C4
d1	Work in a group to achieve final course's project and/or for solving specific problems.	D1
d2	Perform specific tasks individually and present tasks' ideas clearly.	D4

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies		
Course Intended Learning Outcomes	**Teaching strategies**	**Assessment Strategies**
a1- Define the principles, terminologies, and architectures of HDL and FPGA.	Lectures Self-learning Dialogue and discussion	Written Test and Quizzes Oral discussion Assignment
a2- Explain the different methods of HDL applied in designing of digital circuits and systems.	Lectures Laboratory Self-learning Dialogue and discussion	Written Test and Quizzes Reports evaluation Presentations evaluation Oral discussion Assignment

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(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies			
Course Intended Learning Outcomes		**Teaching strategies**	**Assessment Strategies**
b1-	Formulate digitals system that serve complex applications.	Lectures Laboratory Projects	Written Test and Quizzes Reports evaluation Presentations evaluation Assignment
b2-	Analyze data of HDL simulation results for concluding the correct design.		

(C) Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies			
Course Intended Learning Outcomes		**Teaching strategies**	**Assessment Strategies**
c1-	Implement digital circuits/systems using the training kit.	Lectures Laboratory Exercises Simulation tools Projects	Written Test and Quizzes Reports evaluation Observation of performance Presentations evaluation Assignment
c2-	Use HDL editor, simulation and synthesis tools for designing and implementing digital circuits and systems.		

(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies			
Course Intended Learning Outcomes		**Teaching strategies**	**Assessment Strategies**
d1-	Work in a group to achieve final course's project and/or for solving specific problems.	Laboratory Coursework Project	Observation Presentations evaluation
d2-	Perform specific tasks individually and present tasks' ideas clearly.	Laboratory Research	Reports evaluation

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IV. Course Content

A – Theoretical Aspect

Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	Contact hours
1.	Review	a1, b1	• Logic fundamentals • Gates • Latches • Flip-Flops • CLC • SLC	2	4
2.	FPGA	a1	• FPGA architecture • Types • Synthesis	1	2
3.	VHDL or Verilog fundamentals	a1, a2, b1	• Operations • Constructions • Data representation • Formats…etc • Examples.	4	8
4.	Synthesizable code for basic logic components.	a1, a2, b1	• Examples	2	4
5.	Modeling and Simulating	a1, a2, b1	• Modeling • Timing • Events • Propagation delays • Concurrency	2	4
6.	Synthesizable code and hardware/HDL	a1, a2, b1	• Examples	3	6

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	mapping (CLC, SLC).				
Number of Weeks /and Units Per Semester				**14**	**28**

B - Practical Aspect

Order	Topics List	Number of Weeks	Contact hours	Learning Outcomes
1	Identify the editor and simulation programs	1	2	b2, c1, c2
2	FPGA and synthesis methods	1	2	a1, c1, c2
3	VHDL or Verilog fundamentals	3	6	a1, a2, b1, b2, c1, c2, d1
4	Synthesizable code for basic logic components	2	4	a1, a2, b1, b2, c1, c2, d1
5	Modeling and Simulating	2	4	a1, a2, b1, b2, c1, c2, d1
6	Synthesizable code and hardware/HDL mapping (CLC, SLC)	3	6	a1, a2, b1, b2, c1, c2, d1
7	Term Project Presentation and Discussion (Designing and implementing a digital system to serve digital application using HDL) starting from the 3rd week	1	2	a1, a2, b1, b2, c1, c2, d1, d2
8	Final Lab. Exam.	1	2	a1, a2, b1, b2, c1, c2, d2
Number of Weeks /and Units Per Semester		**14**	**28**	

V. Teaching strategies of the course

- Lectures
- Laboratory
- Self-learning
- Dialogue and discussion
- Projects

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- Exercises
- Simulation tools
- Coursework
- Research

VI. Assignments & Reports

No	Assignments	Aligned CILOs	Week Due	Mark
1.	VHDL & Verilog Programming	a2, b1, c1, c2, d2	3rd to 6th	3
2.	Search Report on FPGA, VHDL Simulation and Modeling of Digital Circuits/Systems	a1, a2, b1, c1, c2, d1, d2	8th to 13th	4
3.	Laboratory reports	a2, b1, c1, c2, d2	Weekly	8
	Total			**15**

VII. Schedule of Assessment Tasks for Students during the Semester

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & Reports	Weekly	15	10%	a1, a2, b1, c1, c2, d1, d2
2.	Quizzes	3rd, 6th, and 13th	10	6.67%	a1, a2, b1, b2, c1
3.	Midterm Exam (Theoretically)	8th	20	13.33%	a1, a2, b1, b2, c1
4.	Final Lab. Exam (including Term Project Evaluation)	13th & 14th	30	20%	a1, a2, b1, b2, c1, c2, d1, d2
5.	Final Exam	16th	75	50%	a1, a2, b1, b2
Total			**150**	**100%**	

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Quality Assurance Unit
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Prof. Dr. Mohammed AL-Bukhaiti

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Assoc. Prof. Dr. Huda Al-Emad

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VIII. Learning Resources

Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two)

1) D. J. Smith (1998), HDL chip design: a practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog, Latest Edition, Doone Publications.
2) Weng Fook Lee (2000), VHDL Coding and Logic Synthesis with Synopsys, First Edition, Academic Press.

2- Essential References

1) Michael D. Ciletti (1999), Modeling, Synthesis, and Rapid Prototyping with the Veriog HDL, First Edition. Pearson Prentice Hall.
2) D. Naylor and S. Jones, VHDL: A Logic Synthesis Approach, Chapman & Hall, UK.
3) Thomas L. Floyd, (2006), Digital Fundamentals, Ninth Edition, Pearson Prentice Hall, United States of America.

3- Electronic Materials and Web Sites etc.

Software and Programs: -

1) Quartus program.
2) Mentro Graphics program.

IX.Course Policies:

1.	**Class Attendance:** - The students should have more than 75% of attendance according to rules and regulations of the faculty.
2.	**Tardy**: - The students should respect the timing of attending the lectures. They should attend within 15 minutes from starting of the lecture.
3.	**Exam Attendance/Punctuality:** - The student should attend the exam on time. The punctuality should be implemented according to rules and regulations of the faculty for mid-term exam and final exam.

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4.	**Assignments & Projects:** - The assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time.
5.	**Cheating**: - If any cheating occurred during the examination, the student is not allowed to continue and he has to face the examination committee for enquires.
6.	**Plagiarism**: - If one student attends the exam on another behalf; he will be dismissed from the faculty according to the policy, rules and regulations of the university.
7.	**Other policies:** - All the teaching materials should be kept out the examination hall and mobile phones are not allowed. - Mutual respect should be maintained between the student and his teacher and also among students. Failing in keeping this respect is subject to the policy, rules and regulations of the university.

Reviewed By	**Vice Dean for Academic Affairs and Post Graduate Studies: Asst. Prof. Dr. Tarek A. Barakat** **President of Quality Assurance Unit: Assoc. Prof. Dr. Mohammed Algorafi** **Name of Reviewer from the Department: Assoc. Prof. Dr. Farouk Al-Fuhaidy**
	Deputy Rector for Academic Affairs Asst. Prof. Dr. Ibrahim AlMutaa **Assoc. Prof. Dr. Ahmed Mujahed** **Asst. Prof. Dr. Munasar Alsubri**

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Electrical Engineering Department
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Course Plan of Hardware Design Language

I. Information about Faculty Member Responsible for the Course							
Name of Faculty Member	Prof. Abdul Raqib Abdo Asaad	**Office Hours**					
Location&Telephone No.		**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail							

II. Course Identification and General Information						
1.	Course Title:	Hardware Design Language				
2.	Course Number & Code:	CCE245				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	-	2	-	3
4.	Study level/year at which this course is offered:	Third Year/ First Semester				
5.	Pre –requisite (if any):	Programming Language (II), Logic Circuits (I), Logic Circuits (II)				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered	B.Sc. of Computer and Control Engineering				
8.	Language of teaching the course:	Arabic & English				
9.	System of Study:	Semesters				
10.	Mode of delivery:	Lecture				
11.	Location of teaching the course:	Class Room (Faculty of Engineering)				

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III. Course Description

This course aims to provide students with basic principles, fundamentals and concepts related to the development of digital integrated circuits based on VHDL programming. Modern practices of HDLs using VHDL or Verilog languages for modeling, timing, events, etc. has raised demands and applications in industrial's digital systems evolution and development. Course topics cover review on logic gates, combinational and sequential logic circuits, FPGA, Verilog & VHDL fundamentals and programming and modeling and simulation of ICs. Based on lectures, practical & computer labs and term projects works, students will be able to develop their problem-solving, programming, modeling and simulation skills related to ICs development.

IV. Intended learning outcomes (ILOs) of the course:

1. Define the principles, terminologies, and architectures of HDL and FPGA.
2. Explain the different methods of HDL applied in designing of digital circuits and systems.
3. Formulate digitals system that serve complex applications.
4. Analyze data of HDL simulation results for concluding the correct design.
5. Implement digital circuits/systems using the training kit.
6. Use HDL editor, simulation and synthesis tools for designing and implementing of digital circuits and systems.
7. Work in a group to achieve final course's project and/or for solving specific problems.
8. Perform specific tasks individually and present tasks' ideas clearly.

V. Course Content

A – Theoretical Aspect

Order	Units/Topics List	Sub Topics List	Number of Weeks	Contact hours
1.	Review	• Logic fundamentals • Gates • Latches • Flip-Flops	1st ,2nd	4

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		• CLC • SLC		
2.	FPGA	• FPGA architecture • Types • Synthesis	3rd	2
3.	VHDL or Verilog fundamentals	• Operations • Constructions • Data representation • Formats…etc • Examples.	4th ,5th ,6th ,7th	8
4.	Midterm		8th	2
5.	Synthesizable code for basic logic components.	• Examples	9th ,10th	4
6.	Modeling and Simulating	• Modeling • Timing • Events • Propagation delays • Concurrency	11th ,12th	4
7.	Synthesizable code and hardware/HDL mapping (CLC, SLC).	• Examples	13th ,14th ,15th	6
8.	Final exam	•	16th	2
Number of Weeks /and Units Per Semester			**16**	**32**

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B - Practical Aspect			
Order	**Topics List**	**Number of Weeks**	**Contact hours**
1	Identify the editor and simulation programs	1st	2
2	FPGA and synthesis methods	2nd	2
3	VHDL or Verilog fundamentals	3rd ,4th ,5th	6
4	Synthesizable code for basic logic components	6th ,7th	4
5	Modeling and Simulating	8th ,9th	4
6	Synthesizable code and hardware/HDL mapping (CLC, SLC)	10th ,11th ,12th	6
7	Term Project Presentation and Discussion (Designing and implementing a digital system to serve digital application using HDL) starting from the 3rd week	13th	2
8	Final Lab. Exam.	14th	2
Number of Weeks /and Units Per Semester		**14**	**28**

VI. Teaching strategies of the course

- Lectures
- Laboratory
- Self-learning
- Dialogue and discussion
- Projects
- Exercises
- Simulation tools
- Coursework
- Research

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VII. Assignments & Reports

No	Assignments	Aligned CILOs	Week Due	Mark
1.	VHDL & Verilog Programming	a2, b1, c1, c2, d2	3rd to 6th	3
2.	Search Report on FPGA, VHDL Simulation and Modeling of Digital Circuits/Systems	a1, a2, b1, c1, c2, d1, d2	8th to 13th	4
3.	Laboratory reports	a2, b1, c1, c2, d2	Weekly	8
	Total			**15**

VIII. Schedule of Assessment Tasks for Students during the Semester

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Assignments & Reports	Weekly	15	10%	a1, a2, b1, c1, c2, d1, d2
2.	Quizzes	3rd, 6th, and 13th	10	6.67%	a1, a2, b1, b2, c1
3.	Midterm Exam (Theoretically)	8th	20	13.33%	a1, a2, b1, b2, c1
4.	Final Lab. Exam (including Term Project Evaluation)	13th & 14th	30	20%	a1, a2, b1, b2, c1, c2, d1, d2
5.	Final Exam	16th	75	50%	a1, a2, b1, b2
Total			**150**	**100%**	

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Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

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	Software and Programs: - 1. Quartus program. 2. Mentro Graphics program.

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