Sana'a University
Faculty of Engineering
Electrical Engineering Department
B.Sc. of Computer and Control Engineering

Course Specification of Digital Computer Design

I. Course Identification and General Information

1.	Course Title:	Digital Computer Design				
2.	Course Code &Number:	CCE417				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	-	2	-	3
4.	Study level/ semester at which this course is offered:	Fifth Year/ First Semester				
5.	Pre –requisite (if any):	Computer Architecture and Organization, Digital Systems Design.				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered:	B.Sc. of Computer and Control Engineering				
8.	Language of teaching the course:	Arabic & English				
9.	Location of teaching the course:	Class Room (Faculty of Engineering)				
10.	Prepared By:	Prof. Abdul Raqib Abdo Asaad				
11.	Date of Approval					

II. Course Description

This course concerns on providing students with advanced concepts and principles related to the organization and design of a digital computer. The computer hardware technology is growing fast with rapid change and has variant applications to different environments. Course topics include the organization and design of major components of a digital computer including the CPU, memory, input and output units, the integration of components into a system and the simulation by a computer design language. Throughout lab activities and course work project, students will develop their design and simulation skills for the practice of digital computer system and components to real and/or simulation platforms.

1. Prepared by	Head of Department	Quality Assurance Unit	Dean of the Faculty	Academic Development Center & Quality Assurance
Prof. Abdul Raqib Abdo Asaad	Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Assoc. Prof. Dr. Mohammad Algorafi	Prof. Dr. Mohammed AL-Bukhaiti	Assoc. Prof. Dr. Huda Al-Emad

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III. Course Intended learning outcomes (CILOs) of the course		Referenced PILOs
a1	Clarify the organization and the function of each component in a digital computer as well as their description using RTL.	A1
a2	Define principles and simulation tools applied to the digital computer design.	A2
b1	Compose the CPU and other main units of digital computers.	B1, B4
b2	Analyze data of a VHDL/Verilog simulation results for concluding the correct design.	B2, B3
c1	Design the essential hardware and software components of a digital computer.	C1, C2
c2	Use a VHDL/Verilog editor tool for designing and implementing a digital computer using simulation and synthesis tools.	C3, C4
d1	Work in a group to achieve final course's project or to solve specific problems related to digital computer and component design.	D1
d2	Consider the following of standards to achieve reports and presentations.	D4

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies			
Course Intended Learning Outcomes		**Teaching strategies**	**Assessment Strategies**
a1-	Clarify the organization and the function of each component in a digital computer as well as their description using RTL.	Lectures Dialogue and discussion Laboratory work Self-learning	Written Test and Quizzes Reports evaluation Presentations evaluation Assignment
a2-	Define principles and simulation tools applied to the digital computer design.	Lectures Laboratory work	Written Test and Quizzes Reports evaluation Assignment

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(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies		
Course Intended Learning Outcomes	**Teaching strategies**	**Assessment Strategies**
b1- Compose the CPU and other main units of digital computers.	Lectures Laboratory work Project	Written Test and Quizzes Reports evaluation Presentations evaluation Assignment
b2- Analyze data of a VHDL/Verilog simulation results for concluding the correct design.	Lectures Project Laboratory work	Written Test and Quizzes Reports evaluation Presentations evaluation Assignment

(C) Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies		
Course Intended Learning Outcomes	**Teaching strategies**	**Assessment Strategies**
c1- Design the essential hardware and software components of a digital computer.	Lectures Dialogue and discussion Laboratory work Project Design exercises	Written Test and Quizzes Coursework assignments Reports evaluation Presentations evaluation Assignment
c2- Use a VHDL/Verilog editor tool for designing and implementing a digital computer using simulation and synthesis tools.	Project Laboratory work Design exercises Self-learning	Coursework assignments Reports evaluation Presentations evaluation

(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies		
Course Intended Learning Outcomes	**Teaching strategies**	**Assessment Strategies**
d1- Work in a group to achieve final course's project or to solve specific problems related to	Project Design exercises Self-learning	Coursework assignments Reports evaluation Presentations evaluation

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	digital computer and component design.		
d2-	Consider the following of standards to achieve reports and presentations.	Project Laboratory work Self-learning	Reports evaluation Presentations evaluation

IV. Course Content

A – Theoretical Aspect

Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	Contact hours
1.	Digital computer systems	a1, b1	▪ Type of digital computer systems ▪ Component of a digital computer system	1	2
2.	An Introduction to high-level synthesis using RTL	a1, a2	▪ RTL Terminologies ▪ RTL symbols ▪ RTL rules ▪ RTL examples	2	4
3.	Instruction set design	a2, c1	▪ Type of instructions ▪ Instruction format ▪ Efficiency ▪ Completeness ▪ Regularity	1	2
4.	CPU design	a1, a2, b1, c1	▪ Data path design, ▪ Control unit design, ▪ Register unit design.	3	6
5.	CPU Design (Cont.)	a1, a2, b1, c1	▪ Clock generator design	1	2
6.	Memory & I/O systems design	a1, a2, b1, c1	▪ Memory design ▪ Input/output unit design	2	4
7.	Power supply design	a2, b1, c1	▪ Power supply design	1	2

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8.	Assembler design	a2, c1	▪ One-pass assembler ▪ Two-pass assembler	2	4
9.	Course Project Presentation	a1, a2, b1, b2, c1, c2, d1, d2	▪ Course Project Presentation	1	2
Number of Weeks /and Units Per Semester				**14**	**28**

B - Practical Aspect

Based on Computer and VHDL Labs

Order	Topics List	Number of Weeks	Contact hours	Learning Outcomes
1.	Digital computer systems (Type of digital computer systems, Component of a digital computer system)	1	2	a1, b1, d1
2.	An Introduction to high-level synthesis using RTL (RTL Terminologies, RTL symbols, RTL rules, RTL examples)	2	4	a1, a2, d1
3.	Instruction set design (Type of instructions, Instruction format, Efficiency, Completeness, Regularity)	1	2	a2, c1, d1
4.	CPU design (Data path design, Control unit design, Register unit design, Clock generator design)	4	8	a1, a2, b1, b2, c1, c2, d1, d2
5.	Memory & I/O systems design	2	4	a1, a2, b1, b2, c1, c2, d1
6.	Power supply design	1	2	a2, b1, b2, c1, c2, d1, d2
7.	Assembler design (One-pass assembler, Two-pass assembler)	2	4	a2, c1, d1
8.	Final Lab Exam	1	2	a1, a2, b1, b2, c1, c2
Number of Weeks /and Units Per Semester		**14**	**28**	

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V. Teaching strategies of the course

- Lectures
- Dialogue and discussion
- Laboratory Work
- Self-learning
- Project
- Design exercises

VI. Assignments & Reports

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1.	Assignment on RTL	a1, a2, b1, b2, c1, c2, d1	3rd	2
2.	Research Report on CPU Design using VHDL and New Trends	a1, a2, b1, b2, c1, c2, d1, d2	7th	3
3.	Research Report and Assignment on Memory Design using VHDL and New Technology related to Memory.	a1, a2, b1, b2, c1, c2, d1, d2	11th	3
4.	Lab, Problems and Exercises Reports	a1, a2, b1, b2, c1, c2, d1	3rd to 13th	7
Total Marks				**15**

VII. Schedule of Assessment Tasks for Students during the Semester

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Course project (designing and simulating a small digital computer using VHDL or Verilog language and tools).	15th	22.5	15%	a1, a2, b1, b2, c1, c2, d1, d2

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2.	Assignments & Reports	3rd to 13th	15	10%	a1, a2, b1, b2, c1, c2, d1, d2
3.	Midterm Exam	9th	22.5	15%	a1, a2, b1, c1
4.	Final Lab Exam	14th	15	10%	a1, a2, b1, b2, c1, c2
5.	Final Exam	16th	75	50%	a1, a2, b1, b2, c1
Total			**150**	**100%**	

VIII. Learning Resources

- Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two)

1) Larry L. Wear and others (1991), "Computers: An Introduction to Hardware and Software Design", McGraw Hill Series in Electrical and Computer Engineering.
2) Sajjan G. Shiva (2007), "Computer Organization, Design, and Architecture", Fourth Edition, CRC Press.

2- Essential References

1) V Rajaraman and T. Radhakrishnan (2008), "An introduction to digital computer design", fifth Edition. Prentice-Hall of India.
2) M. Morris R. Mano (1992), "Computer System Architecture", Third Edition, Pearson.
3) W. Stalling, (2003), "Computer Organization & Architecture: Designing for Performance", Prentice Hall.

3- Electronic Materials and Web Sites etc.

IX. Course Policies:

1. **Class Attendance:**

A student should attend not less than 75 % of total hours of the subject; otherwise he/she will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring a proof statement from university

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	Clinic. If the absent is more than 25% of a course total contact hours, student will be required to retake the entire course again.
2.	**Tardy:** For late in attending the class, the student will be initially notified. If he repeated lateness in attending class, he/she will be considered as absent.
3.	**Exam Attendance/Punctuality:** A student should attend the exam on time. He/she is permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam
4.	**Assignments & Projects:** In general one assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time, mostly one week after given the assignment.
5.	**Cheating**: For cheating in exam, a student will be considered as fail. In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.
6.	**Plagiarism**: Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee proofed a plagiarism of a student, he/she will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university or according to the university roles.
7.	**Other policies:** - Mobile phones are not allowed to use during a class lecture. It must be closed; otherwise the student will be asked to leave the lecture room. - Mobile phones are not allowed in class during the examination. - Lecture notes and assignments might be given directly to students using soft or hard copy.

Reviewed By	**Vice Dean for Academic Affairs and Post Graduate Studies: Asst. Prof. Dr. Tarek A. Barakat**

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Prof. Abdul Raqib Abdo Asaad	Asst. Prof. Dr. Adel Ahmed Al-Shakiri	Assoc. Prof. Dr. Mohammad Algorafi	Prof. Dr. Mohammed AL-Bukhaiti	Assoc. Prof. Dr. Huda Al-Emad

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	President of Quality Assurance Unit: Assoc. Prof. Dr. Mohammed Algorafi **Name of Reviewer from the Department: Assoc. Prof. Dr. Farouk Al-Fuhaidy**
	Deputy Rector for Academic Affairs Asst. Prof. Dr. Ibrahim AlMutaa **Assoc. Prof. Dr. Ahmed Mujahed** **Asst. Prof. Dr. Munasar Alsubri**

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Electrical Engineering Department
B.Sc. of Computer and Control Engineering

Course Plan of Digital Computer Design

I. Information about Faculty Member Responsible for the Course							
Name of Faculty Member	Prof. Abdul Raqib Abdo Asaad	**Office Hours**					
Location&Telephone No.		**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail							

II. Course Identification and General Information						
1.	Course Title:	Digital Computer Design				
2.	Course Number & Code:	CCE417				
3.	Credit hours:	C.H				Total
		Th.	Tu.	Pr.	Tr.	
		2	2	-	-	3
4.	Study level/year at which this course is offered:	Fifth Year/ First Semester				
5.	Pre –requisite (if any):	Computer Architecture and Organization, Digital Systems Design.				
6.	Co –requisite (if any):	None.				
7.	Program (s) in which the course is offered	B.Sc. of Computer and Control Engineering				
8.	Language of teaching the course:	Arabic & English				
9.	System of Study:	Semesters				
10.	Mode of delivery:	Lecture.				
11.	Location of teaching the course:	Class Room (Faculty of Engineering)				

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III. Course Description

This course concerns on providing students with advanced concepts and principles related to the organization and design of a digital computer. The computer hardware technology is growing fast with rapid change and has variant applications to different environments. Course topics include the organization and design of major components of a digital computer including the CPU, memory, input and output units, the integration of components into a system and the simulation by a computer design language. Throughout lab activities and course work project, students will develop their design and simulation skills for the practice of digital computer system and components to real and/or simulation platforms.

IV. Intended learning outcomes (ILOs) of the course:

1. Clarify the organization and the function of each component in a digital computer as well as their description using RTL.
2. Define principles and simulation tools applied to the digital computer design.
3. Compose the CPU and other main units of digital computers.
4. Analyze data of a VHDL/Verilog simulation results for concluding the correct design.
5. Design the essential hardware and software components of a digital computer.
6. Use a VHDL/Verilog editor tool for designing and implementing a digital computer using simulation and synthesis tools.
7. Work in a group to achieve final course's project or to solve specific problems related to digital computer and component design.
8. Consider the following of standards to achieve reports and presentations.

V. Course Content

A – Theoretical Aspect

Order	Units/Topics List	Sub Topics List	Number of Weeks	Contact hours
1.	Digital computer systems	▪ Type of digital computer systems ▪ Component of a digital computer system	1st	2
2.	An Introduction to high-level	▪ RTL Terminologies ▪ RTL symbols ▪ RTL rules	2nd ,3rd	4

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	synthesis using RTL	▪ RTL examples		
3.	Instruction set design	▪ Type of instructions ▪ Instruction format ▪ Efficiency ▪ Completeness ▪ Regularity	4th	2
4.	CPU design	▪ Data path design, ▪ Control unit design, ▪ Register unit design.	5th ,6th ,7th	6
5.	Mid-Term Exam	▪ ALL Previous Topics	8th	2
6.	CPU Design (Cont.)	▪ Clock generator design	9th	2
7.	Memory & I/O systems design	▪ Memory design ▪ Input/output unit design	10th ,11th	4
8.	Power supply design	▪ Power supply design	12th	2
9.	Assembler design	▪ One-pass assembler ▪ Two-pass assembler	13th ,14th	4
10.	Course Project Presentation	▪ Course Project Presentation	15th	2
11.	Final Exam	▪ ALL Topics	16th	2
Number of Weeks /and Units Per Semester			**16**	**32**

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B - Practical Aspect			
Based on Computer and VHDL Labs			
Order	**Topics List**	**Number of Weeks**	**Contact hours**
1.	Digital computer systems (Type of digital computer systems, Component of a digital computer system)	1st	2
2.	An Introduction to high-level synthesis using RTL (RTL Terminologies, RTL symbols, RTL rules, RTL examples)	2nd ,3rd	4
3.	Instruction set design (Type of instructions, Instruction format, Efficiency, Completeness, Regularity)	4th	2
4.	CPU design (Data path design, Control unit design, Register unit design, Clock generator design)	5th ,6th ,7th ,8th	8
5.	Memory & I/O systems design	9th ,10th	4
6.	Power supply design	11th	2
7.	Assembler design (One-pass assembler, Two-pass assembler)	12th ,13th	4
8.	Final Lab Exam	14th	2
Number of Weeks /and Units Per Semester		**14**	**28**

VI. Teaching strategies of the course

- Lectures
- Dialogue and discussion
- Laboratory Work
- Self-learning
- Project
- Design exercises

VII. Assignments & Reports

No	**Assignments**	**Aligned CILOs(symbols)**	**Week Due**	**Mark**
1.	Assignment on RTL	a1, a2, b1, b2, c1, c2, d1	3rd	2

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2.	Research Report on CPU Design using VHDL and New Trends	a1, a2, b1, b2, c1, c2, d1, d2	7th	3
3.	Research Report and Assignment on Memory Design using VHDL and New Technology related to Memory.	a1, a2, b1, b2, c1, c2, d1, d2	11th	3
4.	Lab, Problems and Exercises Reports	a1, a2, b1, b2, c1, c2, d1	3rd to 13th	7
Total Marks				**15**

VIII. Schedule of Assessment Tasks for Students during the Semester

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1.	Course project (designing and simulating a small digital computer using VHDL or Verilog language and tools).	15th	22.5	15%	a1, a2, b1, b2, c1, c2, d1, d2
2.	Assignments & Reports	3rd to 13th	15	10%	a1, a2, b1, b2, c1, c2, d1, d2
3.	Midterm Exam	8th	22.5	15%	a1, a2, b1, c1
4.	Final Lab Exam	14th	15	10%	a1, a2, b1, b2, c1, c2
5.	Final Exam	16th	75	50%	a1, a2, b1, b2, c1
Total			**150**	**100%**	

IX. Learning Resources

- Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two)

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3- Electronic Materials and Web Sites etc.	

X. Course Policies:

1.	**Class Attendance:** A student should attend not less than 75 % of total hours of the subject; otherwise he/she will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring a proof statement from university Clinic. If the absent is more than 25% of a course total contact hour, student will be required to retake the entire course again.
2.	**Tardy:** For late in attending the class, the student will be initially notified. If he repeated lateness in attending class, he/she will be considered as absent.
3.	**Exam Attendance/Punctuality:** A student should attend the exam on time. He/she is permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam
4.	**Assignments & Projects:** In general one assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time, mostly one week after given the assignment.
5.	**Cheating**:

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	For cheating in exam, a student will be considered as fail. In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.
6.	**Plagiarism**: Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee proofed a plagiarism of a student, he/she will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university or according to the university roles.
7.	**Other policies:** - Mobile phones are not allowed to use during a class lecture. It must be closed; otherwise the student will be asked to leave the lecture room. - Mobile phones are not allowed in class during the examination. - Lecture notes and assignments might be given directly to students using soft or hard copy.

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