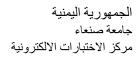




## قائمة الاسئلة معمارية حاسوب - (123103) - المستوى الثالث -تخصص رياضيات - حاسوب - كلية العلوم - الفترة الثانية- درجة الامتحان (30) غالب جمود الحقودي

- 1) 1. What is computer architecture?
  - a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems
  - 2) + b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems
  - 3) c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems
  - 4) d) None of the mentioned
- 2) 2. What is computer organization?
  - 1) + a) structure and behavior of a computer system as observed by the user
  - 2) b) structure of a computer system as observed by the developer
  - 3) c) structure and behavior of a computer system as observed by the developer
  - 4) d) All of the mentioned
- 3) 3. Which of the following is a type of computer architecture?
  - 1) a) Microarchitecture
  - 2) b) Harvard Architecture
  - 3) + c) Von-Neumann Architecture
  - 4) d) All of the mentioned
- 4) 5. Which of the following is the subcategories of computer architecture?
  - 1) a) Microarchitecture
  - 2) b) Instruction set architecture
  - 3) c) Systems design
  - 4) + d) All of the mentioned
- 5) 6. Which of the architecture is power efficient?
  - 1) + a) RISC
  - 2) b) ISA
  - 3) c) IANA
  - 4) d) CISC
- 6) 7. What does CSA stands for?
  - 1) a) Computer Service Architecture
  - 2) + b) Computer Speed Addition
  - 3) c) Carry Save Addition
  - 4) d) None of the mentioned
- 7) 8. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have \_\_\_\_\_
  - 1) a) Generation word
  - 2) b) Exception handling
  - 3) + c) Imprecise exceptions
  - 4) d) None of the mentioned
- 8) 9. To reduce the memory access time, we generally make use of
  - 1) a) SDRAM's
  - 2) b) Heaps
  - 3) + c) Cache's
  - 4) d) Higher capacity RAM's
- 9) 10. The IA-32 system follows which of the following design?
  - 1) + a) CISC

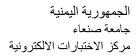
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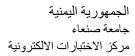
	2)	-	b) SIMD	
	3)	-	c) RISC	
	4)	-	d) None of the mentioned	
10) 11. Which of the following architecture is suitable for a wide range of data types?				
	1)	+	a) IA-32	
	2)	-	b) ARM	
	3)	-	c) ASUS firebird	
	4)	-	,	
11)			2 architecture along with the general flags, which of the following conditional flags are	
	_	ided?	)	
	-	-		
			b) IOPL	
		-		
12)	4)		d) All of the mentioned	
12)			IW architecture follows approach to achieve parallelism.	
			a) SISD	
	3)		b) MIMD c) MISD	
	3) 4)	-	, , , , , , , , , , , , , , , , , , ,	
13)			pes VLIW stands for?	
13)	1)		a) Very Long Instruction Width	
	2)		b) Very Large Instruction Word	
			c) Very Long Instruction Width	
	4)		d) Very Long Instruction Word	
14)			architecture most of the complex instructions are stored in	
	1)	-		
	2)	-	b) Register	
	3)	+	c) Transistors	
	4)	-	d) Diodes	
15)	16. E	Both the	e CISC and RISC architectures have been developed to reduce the	
	1)		· ·	
			b) Semantic gap	
	3)	-	c) Cost	
1.6	4)	-	d) All of the mentioned	
16)	17		are the different type/s of generating control signals.	
	1)		a) Hardwired	
	2) 3)		b) Micro-instruction c) Micro-programmed	
	3) 4)		d) Both Micro-programmed and Hardwired	
17)			all extremely fast, RAM's all called as	
1/)	1)	-	a) Heaps	
	2)		b) Accumulators	
	3)		c) Stacks	
	4)		d) Cache	
18)	,		ven FINITE number of instructions to be executed, which architecture of the processor provides	
,	for a faster execution?			
	1)	-	a) ANSA	
	2)	+	b) Super-scalar	
	3)	-	c) ISA	

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	4)	-	d) All of the mentioned	
19)	20. The interrupt-request line is a part of the			
			a) Data line	
	2)	+	b) Control line	
	3)	-	c) Address line	
	4)	-	d) None of the mentioned	
20)	21.Th	ne retui	rn address from the interrupt-service routine is stored on the	
	1)		a) System heap	
	2)	-	b) Processor register	
	3)	+	c) Processor stack	
			d) Memory	
21)	22. T	he sign	nal sent to the device from the processor to the device after receiving an interrupt is	
	1)	+	a) Interrupt-acknowledge	
	-		b) Return signal	
	3)		c) Service signal	
	4)	-	d) Permission signal	
22)	23.Th	ne time	between the receiver of an interrupt and its service is	
			a) Interrupt delay	
			b) Interrupt latency	
	3)		c) Cycle time	
	4)		d) Switching time	
23) 24.Interrupts form an important part of systems.				
	1)		a) Batch processing	
			b) Multitasking	
			c) Real-time processing	
			d) Multi-user	
24)			ruction, Add #45,R1 does	
			a) Adds the value of 45 to the address of R1 and stores 45 in that address	
			b) Adds 45 to the value of R1 and stores it in R1	
	3)		c) Finds the memory location 45 and adds that content to that of R1	
2.5\	4)	-	d) None of the mentioned	
25)			ressing mode, where you directly specify the operand value is	
			a) Immediate	
	2)		b) Direct	
	3)		c) Definite	
20	4)		d) Relative	
26)			dard SRAM chips are costly as	
	1)		a) They use highly advanced micro-electronic devices	
	2)		b) They house 6 transistor per chip	
	3)		c) They require specially designed PCB's	
27)	4) The 1	- 11	d) None of the mentioned	
21)		ırawba	ck of building a large memory with DRAM is	
	1)	-	a) The large cost factor	
	2)		b) The inefficient memory organisation	
	3)		c) The Slow speed of operation	
287	4)		d) All of the mentioned	
20 <i>)</i>			est data access is provided using a) Caches	
	1.1	-		





- 2) b) DRAM's
- 3) c) SRAM's
- 4) + d) Registers
- 29) 30. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called
  - 1) + a) Level 1 cache
  - 2) b) Level 2 cache
  - 3) c) Registers
  - 4) d) TLB

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