Course Specification of Computer Architecture and Organization

Course No (.....)

2020/2021

Head of Department	Vise Dean for Quality Assurance	Dean of the Faculty	Dean of Academic Development center and Quality
Dr. Ahmed Al-shalabi	Dr. Anwar Al-Shamiri	Dr. Nagi Al-Shibani	Assoc. Prof. Dr.Huda Al.Emad

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Prof. Dr. Qassim Mohammed Abbas

I. Course Identification and General Information:

1	**Course Title:**	**Computer Architecture and Organization**				
2	**Course Code & Number:**					
3	**Credit hours:**	C.H				TOTAL
		Th.	Seminar	Pr	Tr.	
		2		2		3
4	**Study level/ semester at which this course is offered:**	*2nd Year/2nd Semester*				
5	**Pre –requisite (if any):**	Introduction to Computer				
6	**Co –requisite (if any):**	None				
7	**Program (s) in which the course is offered:**	Computer Science				
8	**Language of teaching the course:**	Arabic/English				
9	**Study System**	Term based system				
10	**Mode of delivery:**	Full Time				
11	**Location of teaching the course:**	Faculty of Computer and Information Technology				
12	**Prepared By:**	Dr. Abdul Wasea Al-Azzani				
13	**Date of Approval**					

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II. Course Description:

Computer architecture and organization is the science and art of selecting and interconnecting hardware components to identify a computer that meets functional, performance and cost goals. In this course, you will learn how to a processor computer perform operations, including processor data buses, processor control, pipelining and instruction level parallelism, cache and memory systems, and I/O systems. A practical part of the course provides hands-on experience in upgrading, repairing, and maintaining personal and organization computers. It is a compulsory course.

III. Course Intended learning outcomes (CILOs) of the course		Referenced PILOs A2,A3, B2, C1, D1
a.1	Identify computer system history, components, elements, structures and functions that meet the hardware solution for individual or organization.	**A2, A3**
a.2	Explain CPU operations, bus systems, memory system design and hierarchy, I/O systems, pipelining and instruction level parallelism.	**A3**
a.3	Describe the different instructions of low-level programming language, and using it to solve a specific programming problem.	**A3**
b.1	Combine a computer components and integrate between them to achieve the goals of a cost and performance.	**B2**
b.2	Explore the CPU components and operations, memories technology, bus systems, and a conventional and parallel architectures.	**B2**
b.3	Design simple assembly programs and trace how it interact with computer hardware directly.	**B2**
c.1	Choose appropriate computer components and operate them for individual or organization.	**C1**

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c.2	Practice assembly programming instructions to implement a simple assembler programs and interpret how deal with computer hardware directly.	**C1**
d.1	Work efficiently as a team member or individual to perform a desired task.	**D1**

(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
a1- Identify computer system history, components, elements, structures and functions that meet the hardware solution for individual or organization.	**Lecture, Brainstorming, Exercise, Solve problems in end Chapters, Lab sessions.**	**Mid & Final Semester Exams, Practical Report, Homework.**
a2- Explain CPU operations, bus systems, memor system design and hierarchy, I/O systems, pipelining and instruction level parallelism.	**Lecture, Brainstorming, Exercise, Solve problems in end Chapters, Lab sessions.**	**Mid & Final Semester Exams, Practical Report, Homework.**
a3- Describe the different instructions of low-level programming language, and using it to solve a specific programming problem.	**Lecture, Brainstorming, Exercise, Solve problems in end Chapters, Lab sessions.**	**Mid & Final Semester Exams, Practical Report, Homework.**

(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies:

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Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
b1- Combine a computer components and integrate between them to achieve the goals of a cost and performance.	**Lecture, Brainstorming, Lab Session, Exercise, Problem-Solving in end Chapters.**	**mid & Final Semester Exams, Homework, Practical Report**
b2- Explore the CPU components and operations, memories technology, bus systems, and a conventional and parallel architectures.	**Lecture, Brainstorming, Lab Session, Exercise, Problem-Solving in end Chapters.**	**mid & Final Semester Exams, Homework, Practical Report**
b3- Design simple assembly programs and trace how it interacts with computer hardware directly.	**Lecture, Brainstorming, Lab Session, Exercise, Problem-Solving in end Chapters.**	**mid & Final Semester Exams, Homework, Practical Report**

(C) Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
c1- Choose appropriate computer components and operate them for individual or organization.	**Lecture Notes, Lab Session, Exercise, Problem-Solving in end Chapters.**	**Mid & Final Semester Exams, Practical Report, Homework.**
c2- Practice and use assembly programming instructions and implement a simple assembler programs and interpret how deal with computer hardware directly.	**Lecture Notes, Lab Session, Exercise, Problem-Solving in end Chapters.**	**Mid & Final Semester Exams, Practical Report, Homework.**

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(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies:		
Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
d1- Work efficiently as a team member or individual to perform a desired tasks.	**Lab Session, Exercise, Problem-Solving in end Chapters.**	**Practical Report, Homework.**

I. Course Content:

A – Theoretical Aspect:

Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	contact hours
1	Introduction	a1	• Organization and Architecture • Structure and Function - Function - Structure	1	2
2	Computer Evolution and Performance	a1, b1, b2, c1, d1	• A Brief History of Computers - Computer Generations • Designing for Performance - Microprocessor Speed - Performance Balance - Improvements in Chip Organization and Architecture • The Evolution of the Intel x86 Architecture • Embedded Systems and the ARM	2	4
3	Computer Function and Interconnection	a1, a2, b2, c1, d1	• Computer Components • Computer Function • Instruction Fetch and Execute • Interrupts • I/O Function • Interconnection Structures • Bus Interconnection	2	4

			- Bus Structure - Multiple-Bus Hierarchies - Elements of Bus Design • PCI - Bus Structure - PCI Commands - Data Transfers - Arbitration		
5	**Cache Memory**	a1, a2, b1, b2, c1, d1	• Computer Memory System Overview - Characteristics of Memory Systems - The Memory Hierarchy • Cache Memory Principles • Elements of Cache Design - Cache Addresses - Cache Size - Mapping Function - Replacement Algorithms - Write Policy - Line Size - Number of Caches • Pentium 4 Cache Organization • ARM Cache Organization	2	4
6	**Internal Memory Technology**	a1,a2, b1, b2, c1, d1	• Semiconductor Main Memory Organization - DRAM and SRAM - Types of ROM - Chip Logic - Chip Packaging - Module Organization - Interleaved Memory • Error Correction • Advanced DRAM Organization - Synchronous DRAM - Rambus DRAM - DDR SDRAM - Cache DRAM	2	4
7	**Input/Output**	a1, a2, b1, c1, d1	• External Devices - Keyboard/Monitor - Disk Drive • I/O Modules - Module Function - I/O Module Structure • Programmed I/O	2	4

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			- Overview of Programmed I/O - I/O Commands - I/O Instructions • Interrupt-Driven I/O - Interrupt Processing - Design Issues - Intel 82C59A Interrupt Controller - The Intel 82C55A Programmable Peripheral Interface • Direct Memory Access - Drawbacks of Programmed and Interrupt-Driven I/O - DMA Function • I/O Channels and Processors - The Evolution of the I/O Function - Characteristics of I/O Channels • The External Interface: Firewire and Infiniband - Types of Interfaces - Point-to-Point and Multipoint Configurations - FireWire Serial Bus - InfiniBand		
8	**Computer Arithmetic**	a2, b2, c1, d1	• The Arithmetic and Logic Unit • Integer Representation - Sign-Magnitude Representation - Twos Complement Representation - Converting between Different Bit Lengths - Fixed-Point Representation • Integer Arithmetic - Negation - Addition and Subtraction - Multiplication - Division • Floating-Point Representation - Principles	2	4

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			- IEEE Standard for Binary Floating-Point Representation • Floating-Point Arithmetic - Addition and Subtraction - Multiplication and Division - Precision Considerations - IEEE Standard for Binary Floating-Point Arithmetic		
9	**Parallel Processing**	a2, b1,b2, c1, d1	**Parallel Processing Concepts** **Parallel Processing Classification**	1	2
Number of Weeks /and Units Per Semester				**14**	**28**

B– Practical Aspect: *(if any)*

Order	Topics List	Number of Weeks	Contact Hours
1	**Introduction to computer architecture**	**1**	**2**
2	**Structure of Memory & Registers**	**2**	**2**
3	**X86 instructions (RISC, CISC).**	**3**	**2**
4	**Design first program with Assembly Programming Lang.**	**4**	**2**
5	**I/O instructions set.**	**5**	**2**
6	**Logic instructions set.**	**6**	**2**
8	**Arithmetic instructions set.**	**7**	**2**
9	**Interrupt & Direct Memory access.**	**8**	**2**

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10	Flowchart (jump) instructions set.	9	2
11	Programming Using Various Addressing Modes	10	2
12	Assembly file management	11	2
13	Recursion in Assembly Programming Lang.	12	2
14	To perform interfacing of keyboard controller	13	2
Number of Weeks /and Units Per Semester		13	30

II. Teaching strategies of the course:

Lecture Notes,

Exercises

Problem Solving in end Chapters,

Brainstorming

Labs assignments.

III. Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1	Home work	a1,a2, b2	Monthly	5
2	Problem Solving in end Chapters,	a1,a2, b1,b2, d1	Monthly	5
3	Lab assignments.	a2,a3, b2,b3, c1,c2	Monthly	5

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IV. Schedule of Assessment Tasks for Students During the Semester:

No.	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1	**Assignment**	**Monthly**	**15**	15%	a1,a2,a3, b1,b2,b3, c1,c2, d1
2	**Mid Semester Exam (Theoretical)**	**6th**	10	10%	a1,a2, b1,b2, c1
3	**Mid Semester Exam (Practical)**	**7th**	5	5%	a2,a3, b1,b2,b3, c1,c2
4	**Final Semester Exam (Practical)**	**15th**	10	10%	a2,a3, b1,b2,b3, c1,c2
5	**Final Semester Exam (Theoretical)**	**16th**	60	60%	a1,a2, b1,b2, c1
Final Mark			100	100%	

V. Learning Resources:

1- Required Textbook(s) (maximum two).

1. William Stallings, 2019, Computer Organization And Architecture *Designing For Performance*, 11th Edition, Pearson Education.

2- Essential References.

1. Andrew S. Tanebaum, 2013, structured computer organization, 6th Edition, Pearson Education.
2. John P. Hayes, 1997, Computer Organization & Architecture, 3rd edition, New York McGraw-Hill Companies.
3. Mostafa Abd-El-Barr and Hesham El-Rewini,2005, FUNDAMENTALS OF COMPUTER ORGANIZATION AND ARCHITECTURE, USA, A JOHN WILEY & SONS, INC PUBLICATION.
4. Linda Null; Julia Lobur ,2019 ,The essentials of computer organization and architecture, 5th ed, Jones & Bartlett Learning.

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3-	**Electronic Materials and Web Sites *etc.***
	1. Lecture Notes, 2. WilliamStallings.com/ComputerOrganization 3. ComputerScienceStudent.com 4. https://www.geeksforgeeks.org/computer-organization-and-architecture-tutoria

VI. Course Policies:

1	**Class Attendance:** Class Attendance is mandatory. A student is considered absent and shall be banned from taking the final exam if his/her absence exceeds 25% of total classes.
2	**Tardiness:** A student will be considered late if he/she is not in class after 10 minutes of the start time of class.
3	**Exam Attendance/Punctuality:** No student shall be allowed to the exam hall after 30 minutes of the start time, and shall not leave the hall before half of the exam time has passed.
4	**Assignments & Projects:** Assignments and projects must be submitted on time. Students who delay their assignments or projects shall lose the mark allocated for the same.
5	**Cheating:** Cheating is an act of fraud that results in the cancelation of the student's exam or assignment. If it takes place in a final exam, the penalties stipulated for in the Uniform Students' Bylaw (2007) shall apply.
6	**Forgery and Impersonation:** Forgery/Impersonation is an act of fraud that results in the cancelation of the student's exam, assignment or project. If it takes place in a final exam, the penalties stipulated for in the Uniform Students' Bylaw (2007) shall apply**.**

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7	**Other policies:** The University official regulations in force will be strictly observed and students shall comply with all rules and regulations of the examination set by the Department, Faculty and University Administration.

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Faculty of Computer & Information Technology

Department of Computer Science

Program of Computer Science

Course Specification of Computer Architecture and Organization

Course No (.....)

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2020/2021

Computer Architecture and Organization Course Plan (Syllabus)

I. Information about Faculty Member Responsible for the Course:

		Office Hours					
Name of Faculty Member	Computer and Information Technology (FCIT)						
Location &Telephone No.	Faculty of Computer and Information Technology (FCIT)	**SAT**	**SUN**	**MON**	**TUE**	**WED**	**THU**
E-mail							

II. Course Identification and General Information:

1	**Course Title:**	**Computer Architecture and Organization**				
2	**Course Number & Code:**					
3	**Credit hours:**	**C.H**				**Total**
		Th.	**Seminar**	**Pr.**	**Tr.**	
		2		***2***		***3***
4	**Study level/year at which this course is offered:**	*2nd Year/2nd Semester*				
5	**Pre –requisite (if any):**	Introduction to Computer				

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6	**Co –requisite (if any):**	None
7	**Program (s) in which the course is offered**	Computer Science
8	**Language of teaching the course:**	Arabic/English
9	**System of Study:**	Term based system
10	**Mode of delivery:**	Full Time
11	**Location of teaching the course:**	Faculty of Computer and Information Technology

III. Course Description:

Computer architecture and organization is the science and art of selecting and interconnect hardware components to identify a computer that meets functional, performance and cost goals. In this course, you will learn how to a processor computer perform operations, includ processor data buses, processor control, pipelining and instruction level parallelism, cache a memory systems, and I/O systems. A practical part of the course provides hands-on experie in upgrading, repairing, and maintaining personal and organization computers. It is a compu course.

IV. Intended learning outcomes (ILOs) of the course:

a1. Identify computer system history, components, elements, structures and functions that meet the hardware solution for individual or organization.

a2. Explain CPU operations, bus systems, memory system design and hierarchy, I/O systems, pipelining and instruction level parallelism.

a3. Describe the different instructions of low-level programming language, and using it to solve a specific programming problem.

b1. Combine a computer components and integrate between them to achieve the goals of a cost and performance.

b2. Explore the CPU components and operations, memories technology, bus systems, and a conventional and parallel architectures.

b3. Design simple assembly programs and trace how it interact with computer hardware directly.

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c1. Choose appropriate computer components and operate them for individual or organization.
c2. Practice assembly programming instructions to implement a simple assembler programs and interpret how deal with computer hardware directly.
d1. Work efficiently as a team member or individual to perform a desired task.

V. Course Content:

A – Theoretical Aspect:

Order	Topics List	Week Due	Contact Hours
1	**Introduction:** • **Organization and Architecture** • **Structure and Function** - **Function** - **Structure**	1st	2
2	**Computer Evolution and Performance** • **A Brief History of Computers** - **Computer Generations** • **Designing for Performance** - **Microprocessor Speed** - **Performance Balance** - **Improvements in Chip Organization and Architecture** • **The Evolution of the Intel x86 Architecture** • **Embedded Systems and the ARM**	2nd,3th	4
3	**Computer Function and Interconnection:** • **Computer Components** • **Computer Function** • **Instruction Fetch and Execute** • **Interrupts** • **I/O Function** • **Interconnection Structures** • **Bus Interconnection** - **Bus Structure** - **Multiple-Bus Hierarchies** - **Elements of Bus Design** • **PCI** - **Bus Structure** - **PCI Commands**	4th, 5th	4

	- Data Transfers - Arbitration		
4	**Mid Exam**	6th	2
5	**Cache Memory:** • Computer Memory System Overview - Characteristics of Memory Systems - The Memory Hierarchy • Cache Memory Principles • Elements of Cache Design - Cache Addresses - Cache Size - Mapping Function - Replacement Algorithms - Write Policy - Line Size - Number of Caches • Pentium 4 Cache Organization • ARM Cache Organization	7th, 8th	4
6	**Internal Memory Technology:** • Semiconductor Main Memory Organization - DRAM and SRAM - Types of ROM - Chip Logic - Chip Packaging - Module Organization - Interleaved Memory • Error Correction • Advanced DRAM Organization - Synchronous DRAM - Rambus DRAM - DDR SDRAM - Cache DRAM	9th, 10th	4
7	**Input/Output:** • External Devices - Keyboard/Monitor - Disk Drive • I/O Modules - Module Function - I/O Module Structure • Programmed I/O - Overview of Programmed I/O - I/O Commands - I/O Instructions • Interrupt-Driven I/O - Interrupt Processing	11th, 12th	4

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	- Design Issues - Intel 82C59A Interrupt Controller - The Intel 82C55A Programmable Peripheral Interface • Direct Memory Access - Drawbacks of Programmed and Interrupt-Driven I/O - DMA Function • I/O Channels and Processors - The Evolution of the I/O Function - Characteristics of I/O Channels • The External Interface: Firewire and Infiniband - Types of Interfaces - Point-to-Point and Multipoint Configurations - FireWire Serial Bus - InfiniBand		
8	**Computer Arithmetic:** • The Arithmetic and Logic Unit • Integer Representation - Sign-Magnitude Representation - Twos Complement Representation - Converting between Different Bit Lengths - Fixed-Point Representation • Integer Arithmetic - Negation - Addition and Subtraction - Multiplication - Division • Floating-Point Representation - Principles - IEEE Standard for Binary Floating-Point Representation • Floating-Point Arithmetic - Addition and Subtraction - Multiplication and Division - Precision Considerations - IEEE Standard for Binary Floating-Point Arithmetic	13^{th}, 14^{th}	4
9	**Parallel Processing:** • Parallel Processing Concepts • Parallel Processing Classification	15^{th}	2
10	**Final Exam**	16^{th}	2
Number of Weeks /and Units Per Semester		**16**	**32**

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B– Practical Aspect: *(if any)*			
Order	**Topics List**	**Week Due**	**Contact Hours**
1	Introduction to computer architecture	1st	2
2	Structure of Memory & Registers	2nd	2
3	X86 instructions (RISC, CISC).	3th	2
4	Design first program with Assembly Programming Lang.	4th	2
5	I/O instructions set.	5th	2
6	Logic instructions set.	6th	2
7	Mid exam Lab	7th	2
8	Arithmetic instructions set.	8th	2
9	Interrupt & Direct Memory access.	9th	2
10	Flowchart (jump) instructions set.	10th	2
11	Programming Using Various Addressing Modes	11th	2
12	Assembly file management	12th	2
13	Recursion in Assembly Programming Lang.	13th	2
14	To perform interfacing of keyboard controller	14th	2
15	Final exam Lab	15th	2
Number of Weeks /and Units Per Semester		15	30

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VI. Teaching strategies of the course:

Lecture Notes,
Exercises
Problem Solving in end Chapters,
Brainstorming
Labs assignments.

VII. Assignments:

No	Assignments	Week Due	Mark
1	Exercises	Monthly	5
2	Problem Solving in end Chapters,	Monthly	5
3	Labs assignments.	Monthly	5
Total			15

VIII. Schedule of Assessment Tasks for Students During the Semester:

Assessment	Type of Assessment Tasks	Week Due	Mark	Proportion of Final Assessment
1	Assignment	Monthly	15	15%
2	Mid Semester Exam (Theoretical)	6th	10	10%
3	Mid Semester Exam (Practical)	7th	5	5%

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4	**Final Semester Exam (Practical)**	**15th**	10	10%
5	**Final Semester Exam (Theoretical)**	**16th**	60	60%
Final Mark			100	100%

IX. Learning Resources:

- Written in the following order: (Author – Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two).

1. William Stallings, 2019, Computer Organization And Architecture *Designing For Performance*, 11th Edition, Pearson Education.

2- Essential References.

1. Andrew S. Tanebaum, 2013, structured computer organization, 6th Edition, Pearson Education.
2. John P. Hayes, 1997, Computer Organization & Architecture, 3rd edition, New York McGraw-Hill Companies.
3. Mostafa Abd-El-Barr and Hesham El-Rewini,2005, FUNDAMENTALS OF COMPUTER ORGANIZATION AND ARCHITECTURE, USA, A JOHN WILEY & SONS, INC PUBLICATION.
4. Linda Null; Julia Lobur ,2019 ,The essentials of computer organization and architecture, 5th ed, Jones & Bartlett Learning.

4- Electronic Materials and Web Sites *etc*.

1. Lecture Notes,
2. WilliamStallings.com/ComputerOrganization
3. ComputerScienceStudent.com
4. https://www.geeksforgeeks.org/computer-organization-and-architecture-tutori

X. Course Policies:

Unless otherwise stated, the normal course administration policies and rules of the Faculty of ----- apply. For the policy, see: ----------

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The University Regulations on academic misconduct will be strictly enforced. Please refer to ----------	
1	**Class Attendance:** Class Attendance is mandatory. A student is considered absent and shall be banned from taking the final exam if his/her absence exceeds 25% of total classes.
2	**Tardiness:** A student will be considered late if he/she is not in class after 10 minutes of the start time of class.
3	**Exam Attendance/Punctuality:** No student shall be allowed to the exam hall after 30 minutes of the start time, and shall not leave the hall before half of the exam time has passed.
4	**Assignments & Projects:** Assignments and projects must be submitted on time. Students who delay their assignments or projects shall lose the mark allocated for the same.
5	**Cheating:** Cheating is an act of fraud that results in the cancelation of the student's exam or assignment. If it takes place in a final exam, the penalties stipulated for in the Uniform Students' Bylaw (2007) shall apply.
6	**Forgery and Impersonation:** Forgery/Impersonation is an act of fraud that results in the cancelation of the student's exam, assignment or project. If it takes place in a final exam, the penalties stipulated for in the Uniform Students' Bylaw (2007) shall apply**.**
7	**Other policies:** The University official regulations in force will be strictly observed and students shall comply with all rules and regulations of the examination set by the Department, Faculty and University Administration.

Head of Department	Vise Dean for Quality Assurance	Dean of the Faculty	Dean of Academic Development center and Quality
Dr. Ahmed Al-shalabi	Dr. Anwar Al-Shamiri	Dr. Nagi Al-Shibani	Assoc. Prof. Dr.Huda Al.Emad

Rector of Sana'a University

Prof. Dr. Qassim Mohammed Abbas

اللجنة الإشرافية			
م.	الاســـم	الصـــــفة	التوقيع
١	أ.م.د. عبد الماجد الخليدي	نائب عميد الكلية للشؤون الأكاديمية	
٢	أ.م.د. احمد مجاهد	نائب عميد مركز التطوير الأكاديمي وضمان الجودة	
٣	د. حسين الأشول	ممثل المركز في الكلية	
٤	أ.د. إبراهيم المطاع	نائب رئيس الجامعة للشؤون الأكاديمية	

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