



Course Specification of Digital Logic Design

Course No (.....)

2020/2021

Head of Department	Vise Dean for Quality Assurance	Dean of the Faculty	Dean of Academic Development center and Quality
Dr. Ahmed Al-shalabi	Dr. Anwar Al-Shamiri	Dr. Nagi Al-Shibani	Assoc. Prof. Dr.Huda Al.Emad
Rector of Sana'a University			
Prof. Dr. Qassim Mohammed Abbas			



Course Specification of Digital Logic Design

I. Course Identification and General Information:					
1	Course Title:	Digital Logic Design			
2	Course Code & Number:				
3	Credit hours:	C.H			
		Th.	Seminar	Pr	Tr.
		2	-	2	-
4	Study level/ semester at which this course is offered:	2 nd level, 1 st Semester			
5	Pre –requisite (if any):	None			
6	Co –requisite (if any):	None			
7	Program (s) in which the course is offered:	Computer Science			
8	Language of teaching the course:	English/Arabic			
9	Study System	Term based system			
10	Mode of delivery:	Full time			
11	Location of teaching the course:	Faculty of Computer and Information Technology			
12	Prepared By:	Dr.Anwar Al-Shamiri			
13	Date of Approval				

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II. Course Description:

This course provides the principles of logic design and the basic building blocks used in digital systems, in particular digital computers. It starts with an introduction to the numbering systems, operations on the systems, and the conversion between these systems. The second part discusses the logic gates, Boolean algebra and the gate minimization methods. The third part addresses the combinational logic through the analysis and design of combinational circuits such as adders, subtractors, decoders and multiplexers. The last part will deal with sequential circuits: flip-flops, synthesis of sequential circuits, and case studies, including counters, registers. The course has an accompanying lab component that integrates hands-on experience with modern computer-aided design software including logic simulation and design. Hands-on assignments will make use of tools such as circuit maker, circuit shop, electronic workbench for the design and implementation.

III. Course Intended learning outcomes (CILOs) of the course (maximum 8CILOs)		Referenced PILOs
a1	Show Understanding of the numbering systems and conversion between them	A4
a2	Explore various methods for logic function minimization	
a3	Describe the differences between sequential and combinations logic circuits.	
b1	Differentiate between different logic gates and their functions.	B5
b2	Analyze the combinational and sequential circuits	
b3	Design various combinational and sequential circuits	
c1	Implement combinational and sequential circuits.	C2,C6
c2	Apply the logic principles on the circuit design.	
c3	Use simulation tools to simulate various logic circuits.	
d1	Present solutions to some digital circuits design.	D1,D2

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d2	Work in group analyze and design various realistic problems.	
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(A) Alignment Course Intended Learning Outcomes of Knowledge and Understanding to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
a1. Show Understanding the numbering systems and conversion between them	Lectures, tutorial	Test, Assignments
a2. Define the various methods for logic function minimization	Lectures, tutorial	Test, Assignments
a3. Describe the differences between sequential and combinations logic circuits.	Lectures /Tutorials	Test, Assignments

(B) Alignment Course Intended Learning Outcomes of Intellectual Skills to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
b1. Differentiate between different logic gates and their functions.	Lectures, Lab sessions, Problem solving	Tests, assignments, Case studies
b2. Analyze the combinational and sequential circuits	Lectures, Lab sessions, Problem solving	Tests, assignments, Case studies
b3. Design various combinational and sequential circuits	Lab Sessions, Projects	Tests, assignments, Case studies

© Alignment Course Intended Learning Outcomes of Professional and Practical Skills to Teaching Strategies and Assessment Strategies:

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Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
c1. Implement combinational and sequential circuits.	Tutorial, Lab Sessions, Projects	Tests, Projects, assignments
c2. Apply the logic principles on the circuit design.	Tutorial, Lab Sessions, Projects	Tests, Projects, assignments
c3. Use simulation tools to simulate various logic circuits.	SW Lab sessions, Tutorial	Tests, Projects, assignments

(D) Alignment Course Intended Learning Outcomes of Transferable Skills to Teaching Strategies and Assessment Strategies:

Course Intended Learning Outcomes	Teaching strategies	Assessment Strategies
d1. Present solutions to some digital circuits design.	Seminar , Presentation	Presentation, Report
d2. Work in group analyze and design various realistic problems.	Group learning	Report

IV. Course Content:

A – Theoretical Aspect:

Order	Units/Topics List	Learning Outcomes	Sub Topics List	Number of Weeks	contact hours
1	Numbering systems	a1,c1,d1	Binary, Hex, Octal systems, number Base conversion, Complements, binary codes	2	4

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2	Boolean Algebra and logic gates	a1,b1,c2,d1	Basic theorems of Boolean algebra, Boolean functions, Canonical and standard forms, Logic operations, Digital gates, Integrated circuits.	2	4
3	Gate Level Minimization	a2,c3,d1	SOP,POS (2,3,4) variables simplification Using maps, Don't care conditions,	2	4
5	Combinational logic	a3,b2,c2,c3,d1,d2	Analysis and design procedures of combinational circuits, Adders, subtractors, multipliers, decoders, encoders, multiplexers	3	6
6	Synchronous Sequential Logic	a3,a4,b2,c2,c3,d1,d2	Definition, Latches, Flip-flops, analysis of clocked sequential circuits, state reduction and assignment	3	6
7	Registers and Counters	a4,b3,c2,c3,d1,d2	Registers, Shift Registers, counters, ripples counter, synchronous counters	2	4
Number of Weeks /and Units Per Semester				14	28

B - Practical Aspect: (if any)

Order	Tasks/ Experiments	Number of Weeks	contact hours	Learning Outcomes
1	Solving problems on Numbering systems, conversion, complements.	2	4	a1,b2

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2	Solving book exercise on Boolean algebra theorems.	2	4	a1,b1
3	Solving problems on 2,3,4 k-Map simplification	2	4	a2,c2
4	Explain the LAB simulation software and exercise ICs placement and connections.	2	4	C1,c2,c3,D1,d2
5	Design in Lab various the combinational circuits such as adders, multipliers, decoders, and multiplexers	3	6	A3,b1,c1
7	Design in lab various sequential circuits such as Latches, flip-Flops, ripple counters, decimal counter, up down counters, and shift registers.	3	6	A3,b2,b3c1,c2
Number of Weeks /and Units Per Semester		14	28	

V. Teaching strategies of the course:

- Active lectures
- Tutorials
- presentation Exercises
- Laboratory based session
- Team work
- Problem solving

VI. Assignments:

No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1	Solve some selected questions from chapters 1, 2, and 3	a1,a2,b1,c2,d1,d2	2 nd , 3 rd ,4 th	5

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2	Design of Traffic light	a3,b2,c1,d2	6 th	5
3	Design of lamp handball	a3,b3,c1,c2,c3,d1,d2	10 th	5
4	Design Various counters and registers	a3,b3,c1,c2,c3,d1,d2	12 th	5
Total				20%

VII. Schedule of Assessment Tasks for Students During the Semester:

No	Assessment Method	Week Due	Mark	Proportion of Final Assessment	Aligned Course Learning Outcomes
1	Assignments	2 nd ,3 rd ,4 th ,6 th ,10 th ,12 th	20	20%	a1,a2,a3,b1,b2,b3,c1,c2,c3,d,d2
4	Mid test	12 th	20	20%	a1,a2, ,b1,b2,b3,c1,c2,d1
5	Final exam	16 th	60	60%	a1,a2,a3,b1,b2,b3,c1,c2,c3,d,d2
Total			100	100%	

VIII. Learning Resources:

- Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher).

1- Required Textbook(s) (maximum two).

1. M. Morris Mano & Michael D. Ciletti, 2017, Digital Design with an Introduction to the Verilog HDL, 6th Ed. Pearson
2. Thomas L. Floyd, 2014, Digital Fundamentals, 11th Ed. Pearson

2- Essential References.

1. Jr. Charles H. Roth , Larry L Kinney, 2013, Fundamentals of Logic Design, 7th ed, Cengage Learning.

3- Electronic Materials and Web Sites etc.

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1.	https://www.tutorialspoint.com/digital_circuits/digital_circuits_logic_gate
2.	https://www.electronics-tutorials.ws/

IX. Course Policies:	
Unless otherwise stated, the normal course administration policies and rules of the Faculty of Computer and Information Technology apply. For the policy, see: ----- ----- The University Regulations on academic misconduct will be strictly enforced. Please refer to -----	
1	Class Attendance: A student should attend not less than 75 % of total hours of the subject; otherwise he will not be able to take the exam and will be considered as exam failure. If the student is absent due to illness, he/she should bring a proof statement from university Clinic
2	Tardy: For late in attending the class, the student will be initially notified. If he repeated lateness in attending class he will be considered as absent.
3	Exam Attendance/Punctuality: A student should attend the exam on time. He is Permitted to attend an exam half one hour from exam beginning, after that he/she will not be permitted to take the exam and he/she will be considered as absent in exam.
4	Assignments & Project The assignment is given to the students after each chapter; the student has to submit all the assignments for checking on time.
5	Cheating: For cheating in exam, a student will be considered as fail. In case the cheating is repeated three times during his/her study the student will be disengaged from the Faculty.
6	Plagiarism: Plagiarism is the attending of a student the exam of a course instead of another student. If the examination committee proofed a plagiarism of a student, he will be disengaged from the Faculty. The final disengagement of the student from the Faculty should be confirmed from the Student Council Affair of the university.
7	Other policies: - Mobile phones are not allowed to use during a class lecture. It must be closed, otherwise the student will be asked to leave the lecture room

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	<ul style="list-style-type: none"> - Mobile phones are not allowed in class during the examination. - Lecture notes and assignments my given directly to students using soft or hard copy
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Faculty of Computer & Information Technology

Department of Computer Science

Program of Computer Science

Course Specification of Digital Logic Design

Course No (.....)

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Template for Course Plan (Syllabus)

I. - Information about Faculty Member Responsible for the Course:							
Name of Faculty Member		Office Hours					
Location & Telephone No.		SAT	SUN	MON	TUE	WED	THU
E-mail							

II. Course Identification and General Information:						
1-	2-Course Title:	Digital Logic Design				
3-	4-Course Number & Code:					
5-	6-Credit hours:	C.H				Total
		Th.	Seminar	Pr.	F. Tr.	
		2	-	2		3
7-	8-Study level/year at which this course is offered:	2 nd level- 1 st Semester				
9-	10-Pre –requisite (if any):	None				
11-	12-Co –requisite (if any):	None				
13-	14-Program (s) in which the course is offered	Computer Science				
15-	16-Language of teaching the course:	English/Arabic				
17-	18-System of Study:	Term based system				
19-	20-Mode of delivery:	Full Time				
21-	22-Location of teaching the course:	Faculty of Computer and Information Technology				

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III. Course Description:

This course provides the principles of logic design and the basic building blocks used in digital systems, in particular digital computers. It starts with an introduction to the numbering systems, operations on the systems, and the conversion between these systems. The second part discusses the logic gates, Boolean algebra and the gate minimization methods. The third part addresses the combinational logic through the analysis and design of combinational circuits such as adders, subtractors, decoders and multiplexers. The last part will deal with sequential circuits: flip-flops, synthesis of sequential circuits, and case studies, including counters, registers. The course has an accompanying lab component that integrates hands-on experience with modern computer-aided design software including logic simulation and design. Hands-on assignments will make use of tools such as circuit maker, circuit shop, electronic workbench for the design and implementation.

IV. Intended learning outcomes (ILOs) of the course:

- Brief summary of the knowledge or skill the course is intended to develop:

- a1. Show understanding of the the numbering systems and conversion between them
- a2. Define the various methods for logic function minimization
- a3. Describe the differences between sequential and combinations logic circuits.
- b1. Differentiate between different logic gates and their functions.
- b2. Analyze the combinational and sequential circuits
- b3. Design various combinational and sequential circuits
- c1. Implement combinational and sequential circuits.
- c2. Apply the logic principles on the circuit design.
- c3. Use simulation tools to simulate various logic circuits.
- d1. Present solutions to some digital circuits design.
- d2. Work in group analyze and design various realistic problems.

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V. Course Content:

- Distribution of Semester Weekly Plan of Course Topics/Items and Activities.

A – Theoretical Aspect:

Order	Topics List	Week Due	Contact Hours
1	Numbering systems: Binary, Hex, Octal systems, number Base conversion, Complements, binary codes	2 nd	4
2	Boolean Algebra and logic gates Basic theorems of Boolean algebra, Boolean functions, Canonical and standard forms, Logic operations, Digital gates, Integrated circuits.	4 th	4
3	Gate Level Minimization SOP, POS (2,3,4) variables simplification Using maps, Don't care conditions,	6 th	4
4	First test	7 th	2
5	Combinational logic Analysis and design procedures of combinational circuits, Adders, subtractors, multipliers, decoders, encoders, multiplexers	10 th	6
6	Synchronous Sequential Logic Definition, Latches, Flip-flops, analysis of clocked sequential circuits, state reduction and assignment	13 th	6
7	Registers and Counters Registers, Shift Registers, counters, ripples counter, synchronous counters	15 th	4
8	Final Exam	16 th	2

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Number of Weeks /and Units Per Semester	16	32
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B – Practical Aspect: (if any)			
Order	Topics List	Week Due	Contact Hours
1	Solving problems on Numbering systems, conversion, complements.	3 rd 1 st , 2 nd	4
2	Solving book exercise on Boolean algebra theorems.	3 rd , 4 th	4
3	Solving problems on 2,3,4 k-Map simplification	5 th , 6 th	4
4	Explain the LAB simulation software; exercise ICs, placement and connections.	7 th , 8 th	4
5	Design in Lab the combinational circuits, adders, multipliers, decoders, multiplexers,	9 th -11 th	6
6	First Test	12 th	2
7	Design in lab Latches, flip-Flops, ripple counters, decimal counter, up down counters, shift registers	31 th -15 th	6
8	Evaluation	16 th	2
Number of Weeks /and Units Per Semester		16	32

VI. Teaching strategies of the course:
<ul style="list-style-type: none"> - Active lectures - Tutorials - presentation Exercises - Laboratory based session

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VII. Assignments:				
No	Assignments	Aligned CILOs(symbols)	Week Due	Mark
1	Solve some selected questions from chapters 1, 2, and 3	a1,a2,b1,c2,d1,d2	2 nd , 3 rd ,4 th	5
2	Design of Traffic light	a3,b2,c1,d2	6 th	5
3	Design of lamp handball	a3,b3,c1,c2,c3,d1,d2	10 th	5
	Design Various counters and registers	a3,b3,c1,c2,c3,d1,d2	12 th	5
Total				20%

VIII. Schedule of Assessment Tasks for Students During the Semester:				
Assessment	Type of Assessment Tasks	Week Due	Mark	Proportion of Final Assessment
1	Assignments	2 nd ,3 rd ,4 th ,6 th ,10 th ,12 th	20	20%
2	Mid test	12 th	20	20%
3	Final exam	16 th	60	60%
Total			100	100%

IX. Learning Resources:	
<ul style="list-style-type: none"> Written in the following order: (Author - Year of publication – Title – Edition – Place of publication – Publisher). 	
1- Required Textbook(s) (maximum two).	
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1. Jr. Charles H. Roth , Larry L Kinney, 2013, Fundamentals of Logic Design, 7 th ed, Cengage Learning.
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2. https://www.electronics-tutorials.ws/

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اللجنة الإشرافية			
م.	الاسم	الصفة	التوقيع
١	أ.م.د. عبد الماجد الخليدي	نائب عميد الكلية للشؤون الأكاديمية	
٢	أ.م.د. احمد مجاهد	نائب عميد مركز التطوير الأكاديمي وضمان الجودة	
٣	د. حسين الأشول	ممثل المركز في الكلية	
٤	أ.د. إبراهيم المطاع	نائب رئيس الجامعة للشؤون الأكاديمية	

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