	الجمهورية اليمنية
	جامعة صنعاء
	مركز الاختبارات الالكترونية

| قائمة الاسئلة |
| معمارية و تنظيم الحاسوب -المستوى الرابع -علوم حاسوب - الكل - كلية الحاسوب وتكنولوجيا المعلومات - درجة الامتحان (40) |
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1) The primary difference between computer architecture and computer organization lies in:
1) + The visibility to the programmer
2) - The hardware details
3) - The operational units
4) - The instruction set

2) Architectural attributes have a direct impact on the logical execution of a program.
1) + TRUE.
2) - FALSE.

3) The relationship between a core and a processor is:
1) + A core is a part of a processor
2) - A processor is a part of a core
3) - A core and a processor are the same thing
4) - There is no relationship between a core and a processor

4) The Control Unit contains:
1) - Sequencing logic
2) - Control unit registers
3) - Decoders
4) + All statements are TRUE.

5) The AC (Accumulator) register is used to store the intermediate results of calculations
1) + TRUE.
2) - FALSE.

6) The second generation of computers used:
1) - Transistors
2) - Data channel
3) + Both transistors and data channel
4) - Integrated Circuits

7) Recently, manufacturers (المصنعون) still rely on Moore's Law. to improve computer performance.
1) - TRUE.
2) + FALSE.

8) The future of embedded systems includes:
1) - Increased use of the Internet of Things (IoT)
2) - More powerful and capable embedded systems
3) - Integration with artificial intelligence
4) + All statements are TRUE.

9) Branch prediction and data flow analysis used to increase microprocessor performance are primarily focused on:
1) - Improving the hardware components
2) + Improving the algorithms
3) - Improving the architecture
4) - All statements are TRUE.

10) Superscalar execution can increase the number of instructions executed per clock cycle
1) + TRUE.
2) - FALSE.

11) Increasing the interconnect bandwidth can improve:
1) + Data transfer speed

2)   -   Processor speeds

3)   -   All statements are TRUE.

4)   -   All statements are FALSE.

12) The main difference between Many Integrated Core (MIC) Graphics Processing Unit (GPU):

1)   -   The number of cores

2)   +   The type of tasks they are designed for

3)   -   Their power consumption

4)   -   Their size

13) Determine the address of the next instruction to be executed.

1)   +   Instruction address calculation (iac)

2)   -   Operand address calculation (oac)

3)   -   Instruction fetch (if)

4)   -   Instruction operation decoding (iod)

14) An interrupt service routine (ISR) is:

1)   +   A program that handles interrupts

2)   -   A part of the operating system

3)   -   A hardware component

4)   -   All statements are TRUE.

15) Acknowledges that the pending interrupt has been recognized.

1)   +   Interrupt ACK

2)   -   Interrupt request

3)   -   Bus grant

4)   -   Bus request

16) Computer systems contain many different _____

1)   -   Buses.

2)   -   Lines.

3)   -   Control signal.

4)   +   All statements are TRUE..

17) Primary memory is faster and more expensive than secondary memory.

1)   +   TRUE.

2)   -   FALSE.

18) The physical characteristics of memory can be semiconductor, magnetic, optical, or magneto-optical.

1)   -   TRUE.

2)   +   FALSE.

19) Associative access refers to:

1)   -   Accessing data in a specific linear sequence

2)   -   Accessing data randomly

3)   -   Accessing data directly based on a unique address

4)   +   Accessing data based on a portion of its contents

20) The memory hierarchy is based on the principle that:

1)   -   Faster memory is more expensive.

2)   -   Slower memory is a large.

3)   -   Memory speed and cost are related.

4)   +   All statements are TRUE..

21) If the requested data is not found in the cache, it is called a:

1)   -   Hit

2)   +   Miss
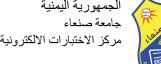
3)   -   Cache line

4)   -   All statements are FALSE..

22) The hardware converts virtual addresses into physical addresses via
1) + Operating system
2) - CPU
3) - Both CPU and operating system.
4) - All statements are FALSE..

23) The main disadvantage of the write-through policy is:
1) + It generates large traffic
2) - It is complex to implement
3) - It reduces the cache hit rate
4) - All statements are FALSE..

24) Permits each main memory block to be loaded into any line of the cache.
1) + Associative Mapping
2) - Direct Mapping
3) - Set Associative
4) - Both Direct and Associative

25) Dynamic RAM (DRAM) requires periodic charge refreshing to:
1) + Maintain data storage
2) - Increase speed
3) - Reduce power consumption
4) - All statements are FALSE.

26) Static RAM (SRAM) uses the same logic elements as:
1) + The processor
2) - The disk
3) - The I/O devices
4) - All statements are FALSE..

27) _____ written into at any time without erasing prior contents.
1) + Electrically erasable programmable read-mostly memory (EEPROM)
2) - Erasable programmable read-mostly memory (EPROM)
3) - Flash Memory
4) - All statements are TRUE..

28) The error correction function has results:
1) - No errors are detected.
2) - An error is detected, and it is possible to correct the error.
3) - An error is detected, but it is not possible to correct it.
4) + All statements are TRUE..

29) Each platter has:
1) + Two surfaces
2) - Three surfaces
3) - Four surfaces
4) - All statements are FALSE..

30) Single-sided disks are more expensive than double-sided disks.
1) - TRUE.
2) + FALSE.

31) The main difference between Solid State Drives (SSD) compared to Hard Disks Drives (HDD) is:
1) - The data transfer rate
2) + The power consumption
3) - All statements are FALSE..
4) - All statements are TRUE..

32) Hard Disks Drives (HDD) use:

1)   -   Flash memory
2)   +   Magnetic disks
3)   -   Optical discs
4)   -   The mixture of glass and ceramic

33)   Addressing modes can be used to:
1)   -   Simplify instruction encoding
2)   -   Improve program efficiency
3)   -   Both Simplify instruction encoding and Improve program efficiency
4)   +   Neither Simplify instruction encoding nor Improve program efficiency

34)   The direct addressing mode is used to:
1)   -   Initialize registers to a constant value
2)   +   Access static data
3)   -   For records implementation
4)   -   All statements are TRUE..

35)   The register indirect addressing mode is like the indirect addressing mode both use to:
1)   -   Initialize registers to a constant value.
2)   -   Handle recursive procedures.
3)   -   All statements are FALSE..
4)   +   Pass an array as a parameter.

36)   The address field references the main memory address and the referenced register contains a positive displacement from that address.
1)   +   Indexing addressing.
2)   -   Base-register addressing.
3)   -   Stack addressing.
4)   -   Relative addressing.

37)   The Complementer is used for:
1)   +   Performing arithmetic operations
2)   -   Performing logical operations
3)   -   Shifting data left or right
4)   -   Controlling the flow of data

38)   Used by the control unit to control the operation of the processor.
1)   +   Control Registers
2)   -   User-Visible Registers
3)   -   Program Status Word (PSW)
4)   -   All statements are TRUE.

39)   Conditional branch instructions can:
1)   -   Improve pipelining performance
2)   +   Limit pipelining performance
3)   -   Do not affect pipelining performance
4)   -   Produces an incorrect result.

40)   Types of pipeline hazards:
1)   -   Resource
2)   -   Data
3)   -   Control
4)   +   All statements are TRUE..