قائمة الاسئلة

معمارية وتنظيم الحاسوب - المستوى الثاني -قسم امن سيبراني - - كلية الحاسوب وتكنولوجيا المعلومات - الفترة - درجة الامتحان (40)

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1) The significant benefits by exploiting locality in computer systems are: ……..
   1) + reduced memory access time, reduced memory bandwidth requirements, lower power consumption, enhanced system responsiveness.
   2) - increased memory bandwidth requirements, more power consumption, enhanced system responsiveness.
   3) - reduced memory access time, increased memory bandwidth requirements, lower power consumption, reduced system responsiveness.
   4) - minimized memory access time, lower power consumption, reduced system responsiveness.
2) An example(s) temporal locality are ……..
   1) - accessing array elements, instruction fetches, loops
   2) - loops, function calls, accessing array elements, instruction fetches,
   3) - function calls, variables, accessing array elements, loops
   4) + loops, function calls, variables
3) The processor registers managed by……..
   1) - processor hardware
   2) + compiler
   3) - dynamic instruction
   4) - operating system
4) Three principles guide the design of a memory hierarchy and the supporting memory management hardware and software: …….
   1) - cost per bit, locality, inclusion
   2) + locality, inclusion, coherence
   3) - locality, inclusion, speed, capacity
   4) - cost per bit, speed, capacity
5) The principle of locality is a fundamental concept in computer architecture, especially in the ……...
   1) - operating system
   2) + design and operation of cache memory
   3) - design and operation of main memory
   4) - compiler design
6) The von Neumann architecture is based on which concept?
   1) - data and instructions are stored in a single read-write memory
   2) - the contents of this memory are addressable by location
   3) - execution occurs in a sequential fashion
   4) + all of the above
7) The interconnection structure in computer system must support which transfer?
   1) - memory to processor
   2) - processor to memory
   3) - I/O to or from memory
   4) + all of the above
8) The data lines provide a path for moving data among system modules and are collectively called the ……..
   1) - control bus
   2) - address bus
   3) + data bus

4) - system bus

9) A …… is the high-level set of rules for exchanging packets of data between devices.
1) - bus
2) + protocol
3) - packet
4) - QPI

10) A(n) …… is generated by execute an illegal machine instruction.
1) - I/O interrupt
2) - hardware failure interrupt
3) - timer interrupt
4) + program interrupt

11) A(n) …… allows the operating system to perform certain functions on a regular basis.
1) - I/O interrupt
2) - hardware failure interrupt
3) + timer interrupt
4) - program interrupt

12) A(n) …… is generated by a signal normal completion of an operation.
1) + I/O interrupt
2) - hardware failure interrupt
3) - timer interrupt
4) - program interrupt

13) A(n) …… is generated by request service from the processor.
1) + I/O interrupt
2) - hardware failure interrupt
3) - timer interrupt
4) - program interrupt

14) The ……. connects major computer components (processor, memory, I/O).
1) - data bus
2) + system bus
3) - data line
4) - control bus

15) In QPI, a …… eliminated the need for arbitration found in shared transmission systems.
1) - layered protocol architecture
2) - packetized data transfer
3) - higher latency
4) + multiple direct connections

16) …….. enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.
1) + Pipelining
2) - Branch prediction
3) - Speculative execution
4) - Superscalar execution

17) In ……, multiple parallel pipelines are used.
1) - pipelining
2) - data flow analysis
3) - speculative execution
4) + superscalar execution

18) In …….., instructions are scheduled to be executed when ready, independent of the original program order.

1) - pipelining
2) + data flow analysis
3) - speculative execution
4) - superscalar execution

19) 1. The approache(s) to achieving increased processor speed is(are): ……
1) + increase the hardware speed of the processor, increase the size and speed of caches, make changes to the processor organization and architecture
2) - increase the hardware speed of the processor, increase the size and speed of main memory
3) - increase the size and speed of main memory
4) - increasing resistance and capacitance, increasing power

20) 2. The desktop application(s) that require the great power of today's microprocessor-based systems include …….
1) - image processing
2) - speech recognition
3) - videoconferencing
4) + all of the above

21) 3. …….. law deals with the potential speedup of a program using multiple processors compared to a single processor.
1) - Moore's
2) + Amdahl's
3) - Little's
4) - Murphy's

22) One increment, or pulse, of a clock is referred to as a …….
1) + clock cycle
2) - clock rate
3) - clock speed
4) - cycle time

23) The …… strategy involves a homogeneous collection of general-purpose processors on a single chip.
1) - graphics processing units (GPUs) and many integrated core (MIC)
2) - multicore and graphics processing units (GPUs)
3) - multicore and general-purpose computing on GPUs (GPGPU)
4) + multicore and many integrated core (MIC)

24) ……. is the fundamental building block of digital circuits used to construct processors, memories, and other digital logic devices.
1) - A gate
2) - The memory cell
3) + The transistor
4) - A thin wafer of silicon

25) …….. is a device that can store one bit of data, and can be in one of two stable states at any time.
1) - A gate
2) + The memory cell
3) - The transistor
4) - A thin wafer of silicon

26) …….. is divided into a matrix of small areas, each a few millimeters square.
1) - A gate
2) - The memory cell
3) - The transistor
4) + A thin wafer of silicon

27) The basic idea behind developing …… is to decrease the average spacing between ICs in an electronic system.
1) + multichip module (MCM) technology
2) - multi-control module (MCM) technology
3) - multichip model (MCM) technology
4) - memory cell module (MCM) technology

28) The ……. is the most widely used for nonembedded computer systems.
1) - ARM architecture
2) - IBM 360 architecture
3) + x86 architecture
4) - AMD architecture

29) The ……. is arguably the most widely used embedded processor, used in cell phones, iPods, remote sensor equipment, and many other devices.
1) + ARM architecture
2) - IBM 360 architecture
3) - x86 architecture
4) - AMD architecture

30) A ……. is a single piece of semiconducting material, typically silicon, upon which electronic circuits and logic gates are fabricated.
1) - multichip module
2) + chip
3) - printed circuit board
4) - gate

31) RISC refers/stand to ……
1) - reduced interruption set computer
2) - reduced information set computer
3) - reduced interruption system computer
4) + reduced instruction set computer

32) The arithmetic and logic unit (ALU) registers include ……...
1) + accumulator register, multiply-quotient register, memory buffer register
2) - program counter, memory address register, instruction register
3) - accumulator register, instruction buffer register, program counter
4) - program counter, memory address register, instruction register, program counter

33) The embedded system examples include ……
1) + cell phones, video cameras, printers
2) - laptops, printers, digital cameras
3) - cell phones, video cameras, desktop computers
4) - laptops, washing machines, lighting systems

34) The …… is primarily driven by deeply embedded devices.
1) - cloud computing
2) - computer network
3) - embedded system
4) + Internet of things (IoT)

35) with ……, you get economies of scale, professional network
1) - management, and professional security management.
2) + cloud computing
3) - computer network
4) - embedded system

36) The …… are examples of computer architectural attributes.

1) + number of bits used to represent various data types, I/O mechanisms, instruction set
2) - memory technology used, interfaces between the computer and peripherals
3) - I/O mechanisms, control signals, memory technology used, techniques for addressing memory
4) - number of bits used to represent various data types, control signals

37) The control unit (CU) registers include ……...
1) - accumulator register, multiply-quotient register, memory buffer register
2) - accumulator register, instruction buffer register, program counter
3) - program counter, memory address register, instruction register, program counter
4) + program counter, memory address register, instruction register

38) CISCs refers/stand to ……
1) - computer instruction set controls
2) + complex instruction set computers
3) - control instruction system computers
4) - computer information set controls

39) The term …….. refers to the use of electronics and software within a product.
1) - computer system
2) + embedded system
3) - memory system
4) - control system

40) The most important in the ……. is the use of data channels.
1) - first generation
2) + second generation
3) - third generation
4) - fourth generation

41) For any given instruction cycle, some states may be null and others may be visited more than once. The states can be implemented in following order: ……
1) - iac, of, oac, if, iod, do, os
2) - if, oac, of, iac, iod, do, os
3) + iac, if, iod, oac, of, do, os
4) - iac, if, oac, of, do, iod, os

42) The instruction fetch cycle includes the following states: ……
1) + Instruction fetch, increments the PC, fetched instruction is loaded into MBR, IBR, and then to IR.
2) - Instruction fetch, instruction decoding operation, fetched instruction is loaded into IR, increments the PC.
3) - Instruction fetch, fetched instruction is loaded into IR, operand address calculation, increments the PC.
4) - Instruction fetch, increments the PC, fetched instruction is loaded into MBR, data operation.

43) The significant characteristics of QPI and other point-to-point interconnect schemes are: …….
1) - multiple direct connections, shared transmission medium, higher latency, and higher data rate.
2) - layered protocol architecture, packetized data transfer, shared transmission medium, and better scalability.
3) - multiple direct connections, layered protocol architecture, shared transmission medium, and higher latency.
4) + multiple direct connections, layered protocol architecture, packetized data transfer, and better scalability.

44) The PCIe protocol architecture encompasses the following layers: ……..
1) - Physical layer, Link layer, Routing layer, Protocol layer.
2) - Physical layer, Routing layer, Transaction layer.

3) + Physical layer, Data link layer, Transaction layer.
4) - Physical layer, Data link layer, Routing layer, Transaction layer.

45) In ……..: Instructions that appear in the execution trace of a program.
1) - Static instruction
2) - Compiler
3) + Dynamic instruction
4) - Operating system

46) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

The address length is ….....

1) - 39 bits
2) - 30 bits
3) - 32 bits
4) + 29 bits

47) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Number of addressable units are …….

1) - 2^{32}bytes
2) - 2^{39} bytes
3) + 2^{29} bytes
4) - 2^{30}bytes

48) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Block size of main memory is ……..

1) - 2^{4} bytes
2) - 2^{8} bytes
3) - 2^{6} bytes
4) + 2^{7} bytes

49) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Number of blocks in main memory = …….

1) + 2^{22} blocks
2) - 2^{27} blocks
3) - 2^{25} blocks
4) - 2^{29}blocks

50) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each.

According to these characteristics, answer the following questions:
Assume an associative mapped cache, the number of lines in cache = …...

1) - $= 2^{16}$ lines
2) - $= 2^{17}$ lines
3) - $= 2^{18}$ lines
4) + all false

51) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a direct mapped cache, the number of lines in cache = …...

1) - 2^{17} lines
2) - 2^{8}lines
3) - 2^{12} lines
4) + 2^{10} lines

52) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a direct mapped cache, the tag size = …...

1) - 15 bits
2) - 10 bits
3) + 12 bits
4) - 14 bits

53) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume an associative mapped cache, the size of the word field is …...

1) - 10 bits
2) - 4 bits
3) + 7 bits
4) - 8 bits

54) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume an associative mapped cache, the size of tag = …...

1) - 23 bits
2) - 21 bits
3) + 22 bits
4) - 20 bits

55) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the number of lines in set = ... Lines.

1) - 8 Lines
2) + 4 Lines
3) - 16 Lines
4) - 2 Lines

56) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the number of lines in cache = ... Lines

1) + 2^{10} lines
2) - 2^{12}lines
3) - 2^{11} lines
4) - 2^{15} lines

57) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the number of sets is .....

1) + 256
2) - 1024
3) - 4096
4) - 512

58) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the size of tag = ...

1) + 14 bits
2) - 9 bits
3) - 16 bits
4) - 11 bits

59) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each. According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the cache line size .....

1) - = 2^{18} bytes
2) - = 2^{16} bytes
3) + = 2^{7} bytes
4) - = 2^{4}bytes

60) Consider a computer system uses a 512 MB main memory with each byte directly addressable, the cache can hold 128 kB, and data are transferred between main memory and the cache in blocks of 128 bytes each.

According to these characteristics, answer the following questions:

Assume a four-way set-associative mapped cache, the cache size …….

1) - $= 2^{16}$bytes
2) + $= 2^{17}$ bytes
3) - $= 2^{18}$bytes
4) - $= 2^{15}$ bytes